T668 MLB

PAGE	CSA	CONTENTS	SYNC	DATE
1	1	TABLE OF CONTENTS		
2	2	REFERENCE DESIGN SYNC TABLES	T668_MLB	07/17/2019
3	4	PD PARTS	T668_KSAITO_MLB_0.11.1	
4	5	SOC: Support	T585_REF_SOC_H13G_0.56.0	
5	6	SOC: CIO, USB, RESETS, CLOCKS, SWD	AITKEN_T668_MLB	10/08/2019
6	7	SOC: AP I/Os	T585_REF_SOC_H13G_0.56.0	
7	8	SOC: LPDP & MIPI	AITKEN_T668_MLB	10/08/2019
8	9	SOC: PCIE	ANDREW_T668_MLB	10/09/2019
9	10	SOC: AOP	T585_REF_SOC_H13G_0.56.0	
10	11	SOC: POWER (DDR,SRAM)	T585_REF_SOC_H13G_0.56.0	
11	12	SOC: POWER (IO)	T585_REF_SOC_H13G_0.56.0	
12	13	SOC: POWER (SOC, CPU, GPU)	T585_REF_SOC_H13G_0.56.0	
13	14	SOC: POWER (SRAM)	T585_REF_SOC_H13G_0.56.0	
14	15	SOC: POWER (Fixed, PLL's, Filtered)	T585_REF_SOC_H13G_0.56.0	
15	16	SOC: GND	T585_REF_SOC_H13G_0.56.0	
16	17	SOC: GND-2	T585_REF_SOC_H13G_0.56.0	
17	19	SPI NOR	REF_SOC_H13G	01/27/2020
18	21	PROJECT SUPPORT (1/2)	AITKEN_T668_MLB	09/18/2019
19	22	PROJECT SUPPORT (2/2)	AITKEN_T668_MLB	11/11/2019
20	50	Secure Element	REF_SE_CERES	02/26/2020
21	51	BATTERY CONNECTORS	AITKEN_T668_MLB	09/18/2019
22	52	PBUS SUPPLY & BATTERY CHARGER	REF_CHARGER_SUONA	02/25/2020
23	53	BATTERY CHARGER SUPPORT	REF_CHARGER_SUONA	04/01/2020
24	57	POWER: 3V8 AON (1/2)	REF_VR_ICEMAN	04/09/2020
25	58	POWER: 3V8 AON (2/2)	REF_VR_ICEMAN	03/30/2020
26	59	POWER: 3V8 AON SUPPORT	T585_REF_VR_ICEMAN_0.36.0	
27	77	PMU: SLAVE INPUT PWR & BUCKS	KEI_T668_MLB	04/07/2020
28	78	PMU: SLAVE LDO	KEI_T668_MLB	04/07/2020
29	79	PMU: SLAVE GPIO & GND	KEI_T668_MLB	04/07/2020
30	80	PMU: SLAVE SUPPORT	KEI_T668_MLB	01/27/2020
31	81	PMU: MASTER INPUT PWR & BUCKS	KEI_T668_MLB	04/02/2020
32	82	PMU: MASTER BUCKS & GND	KEI_T668_MLB	04/26/2020
33	83	PMU: MASTER LDO & GPIO	KEI_T668_MLB	04/23/2020
34	84	PMU: MASTER SUPPORT	KEI_T668_MLB	04/16/2020
35	121	POWER: EXTERNAL LDO	KEI_T668_MLB	09/23/2019
36	123	POWER: 5V S2	REF_VR_5V_TPS62135	04/16/2020
37	124	POWER: 5V S2 SUPPORT	T668_MLB	03/26/2020
38	127	POWER: 3V3 S2	REF_VR_3V3_TPS62135	01/09/2020
39	128	POWER: FETS	KEI_T668_MLB	09/10/2019
40	129	POWER: SUPPORT	KEI_T668_MLB	09/10/2019
41	130	I2C: SIO, DISP	T668_MLB	06/20/2019
42	131	I2C: ISP, AOP	T668_MLB	06/20/2019
43	132	I2C: SMC	KEI_T668_MLB	12/20/2019
44	135	SENSORS: POWER HIGH SIDE (1/2)	KEI_T668_MLB	04/04/2020
45	136	SENSORS: POWER HIGH SIDE (2/2)	KEI_T668_MLB	03/10/2020
46	138	SENSORS: POWER LOW SIDE (1/2)	KEI_T668_MLB	03/10/2020
47	139	SENSORS: POWER LOW SIDE (2/2)	KEI_T668_MLB	01/23/2020
48	140	SENSORS: POWER SUPPORT	KEI_T668_MLB	02/04/2020
49	141	SENSORS: THERMAL (1/2)	KEI_T668_MLB	04/02/2020
50	142	SENSORS: THERMAL (2/2)	KEI_T668_MLB	01/23/2020
51	144	SENSORS: MOTION	WUDI_T668_MLB	09/23/2019
52	145	FAN	AITKEN_T668_MLB	09/18/2019
53	150	USB-C: High Speed ATC0	REF_USBC_ACE2	02/14/2020
54	151	USB-C: High Speed ATC1	REF_USBC_ACE2	02/14/2020
55	152	USB-C: Support 1 ATC01	REF_USBC_ACE2	02/01/2020
56	153	USB-C: Support 2 ATC01	REF_USBC_ACE2	02/01/2020
57	154	USB-C: Port Controller ATC0	REF_USBC_ACE2	02/01/2020
58	155	USB-C: Port Controller ATC1	REF_USBC_ACE2	02/01/2020
59	156	USB-C: Connector(s)	KEI_T668_MLB	02/01/2020
60	157	USB-C: HS Level Shifters	REF_USBC_ACE2	02/04/2020
61	158	USB-C: SUPPORT	T585_REF_USBC_ACE2_0.23.0	
62	200	WIFI/BT: MODULE	REF_WIRELESS_RASPUTIN	02/01/2020
63	201	WIFI/BT: ANTENNA and GND	REF_WIRELESS_RASPUTIN	02/01/2020
64	220	STORAGE: SSD0 S5E <0>	REF_STORAGE_S5E	04/27/2020
65	221	STORAGE: SSD0 S5E <1>	REF_STORAGE_S5E	04/27/2020
66	224	STORAGE: NON OCARINA SUPPORT	REF_STORAGE_NON_OCARINA_SUPPORT	02/25/2020
67	230	STORAGE: SSD SUPPORT	WUDI_T668_MLB	01/28/2020
68	231	SECDIS: MIPI MUX	T585_REF_SECDIS_MIPIMUX_0.7.0	
69	236	DISPLAY: CONNECTOR, PWR	AITKEN_T668_MLB	10/02/2019
70	237	DISPLAY POWER SEQUENCER	REF_PANELPWR_BNJ	04/22/2020
71	238	BEN: CONTROLLER	REF_BLC_BEN	11/21/2019
72	239	BEN: KEYBOARD	REF_BLC_BEN	11/21/2019
73	242	SECDIS: AMR	T585_REF_SECDIS_AMR_0.9.0	
74	243	SECDIS: FPGA	REF_SECDIS_SAK	04/22/2020
75	244	AUDIO SUPPORT	REF_SPKRAMP_TAS5770	04/16/2020
76	245	AUDIO JACK CODEC	REF_CODEC_CLIFDEN	04/13/2020
77	246	AUDIO AMPLIFIERS (1/2)	REF_SPKRAMP_TAS5770	04/16/2020
78	247	AUDIO AMPLIFIERS (2/2)	REF_SPKRAMP_TAS5770	04/16/2020
79	248	AUDIO CONNECTORS: AMPS	KELVIN_T668_MLB	09/18/2019
80	249	AUDIO CONNECTORS: DMIC, JACK	KELVIN_T668_MLB	09/24/2019
81	250	KEYBOARD BLC CONNECTORS	T668_MLB	05/16/2019
82	251	KEYBOARD IOX, SUPPORT	REF_KBD_SUPPORT	02/01/2020
83	252	KEYBOARD SIGNAL CONNECTOR, ESD	WUDI_T668_MLB	01/28/2020
84	253	TRACKPAD SUPPORT	WUDI_T668_MLB	04/16/2020
85	254	TRACKPAD CONNECTOR	WUDI_T668_MLB	04/16/2020
86	256	TOUCHID SUPPORT	T585_REF_MESA_SUPPORT_0.11.0	
87	257	DFR SUPPORT 1	T585_REF_DFR_V3_SUPPORT_0.25.0	
88	258	DFR SUPPORT 2	T585_REF_DFR_V3_SUPPORT_0.25.0	
89	266	FCT	KELVIN_T668_MLB	01/29/2020
90	270	DEBUG: BUTTONS	T668_MLB	06/20/2019
91	271	DEBUG: MISC	T668_MLB	06/20/2019
92	278	DEBUG: LEDS (1/3)	T668_MLB	07/24/2019
93	279	DEBUG: LEDS (2/3)	T668_MLB	07/24/2019
94	280	DEBUG: LEDS (3/3)	T668_MLB	07/24/2019
95	282	DEBUG: P3V8AON ISENSE	T668_MLB	06/20/2019
96	294	DEBUG: VITAMIN-C	MANAN_T668_MLB	02/03/2020
97	300	DESENSE (1/3)	KEI_T668_MLB	11/04/2019
98	301	DESENSE (2/3)	KEI_T668_MLB	09/30/2019
99	302	DESENSE (3/3)	KEI_T668_MLB	09/30/2019
100	310	EMC	KEI_T668_MLB	10/02/2019
101	400	POWER ALIASES 1	KEI_T668_MLB	11/06/2019
102	401	POWER ALIASES 2	KEI_T668_MLB	11/06/2019
103	402	POWER ALIASES 3	T668_MLB	06/05/2019
104	403	POWER ALIASES 4	KEI_T668_MLB	11/06/2019
105	404	POWER ALIASES 5	KEI_T668_MLB	09/12/2019
106	405	SIGNAL ALIASES 1	AITKEN_T668_MLB	09/18/20 9
107	406	SIGNAL ALIASES 2	T668_MLB	05/29/2019
108	500	17.2 RULES	T668_MLB	05/13/2019
109	501	17.2 PHYSICAL CSETS	T668_MLB	05/13/2019
110	502	17.2 SPACING CSETS, ISO	T668_MLB	05/13/2019
111	503	17.2 SPACING CSETS, CLASS-CLASS	T668_MLB	05/13/2019
112	600	BOM VARIANT TABLES	T668_MLB	06/05/2018
113	601	BOM OPTION TABLES	T668_MLB	06/05/2018
114	602		T668_MLB	06/05/2018
115	610	BOM ALTERNATES	T668_MLB	06/05/2018
116	700		T668_MLB	06/05/2018
117	999	CHECKPLUS SUPPORT	T668_MLB	08/29/2019

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REFERENCE DESIGNS J293 SYNCS FROM

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
T585	REF_VR_ICEMAN	57,58	1.14.0		2020/04/27
T585	REF_CHARGER_SUONA	52,53	0.36.0		2020/04/27
T585	REF_STORAGE_NON_OCARINA_SUPPORT	224	0.5.0		2020/04/27
T585		245	1.6.0		2020/04/27
T585	REF_SPKRAMP_TAS5770	244,246,247	0.8.0		2020/04/27
T585	REF_VR_3V3_TPS62135	127	0.8.0		2020/04/27
T585	REF_VR_5V_LT8642S	123	0.13.0		2020/04/27
T585	REF_SECDIS_MIPIMUX	231	0.7.0		2020/04/27
T585	REF_DFR_V3_SUPPORT	257,258	0.25.0		2020/04/27
T585	REF_SE_CERES	50	0.13.0		2020/04/27
T585	REF_PANELPWR_BNJ	237	0.9.0		2020/04/27
	REF_SECD S_ AK	243	40.0		2 20/04/27
T585	REF_STORAGE_S5E	220,221	0.34.0		2020/04/27

REFERENCE DESIGNS NO LONGER SYNCS FROM

SOUR E PROJECT	SUB-DES GN N ME	SUB-DESIGN P G S	VERSION	HARD/ SOFT	YNC_DATE/TIME	
T585	REF_SOC_H13G	5-17,19				<-- WE STOPPED SYNCING SOC AT 0.56.0 DUE TO REF DESIGN DESENSE CAP ADDITIONS CONFLICTING WITH DESENSE TEAM'S REQUESTS FOR J293
T585	REF_PMU_SERA_SIMETRA	77-79,81-83				<-- WE STOPPED SYNCING PMU AT 0.57.0 DUE TO SLOW UPDATES AND REF DESIGN IS OFF GRID
T585	REF_BLC_BEN	238,239				<-- WE STOPPED SYNCING BLC AT 0.16.0 TO RELAX PLACE NEARS
T585	REF DEBUG_STUFF	294				<-- WE STOPPED SYNCING VITAMIN C AT 0.1.0 SINCE THE REF DESIGN IS INCOMPLETE ND MANY CHANGES ARE NEEDED TO SUPPORT VIT C MK II
T585	REF_SECDIS_AMR	242				<-- WE STOPPED SYNCING AMR REF SINCE THE REF HAS A DIFFERENT APN FOR AMR FOOTPRINT THAN PD USES IN J293'S MCO
T 85	REF_USBC_ACE2	150-155,157				<-- WE STOPPED SYNCING USB AT 0.31.0 AS THE 50V CC CAPS WHICH ARE 2.8X MORE EXPENSIVE THAN THE 25V ONES, ALSO LSF0 02 COMBO ADDED
T585	REF_WIRELESS_ ASPUTIN	200-201				<-- WE STOPPED SYNCING RASPUTIN TO ADD RF CONN BOM OPT ON, CHANGE 100M CLK TPS TO PPS, AND FIX OVERLAPPING IPU TEXT NOTES
T585	REF_MESA_SUPPORT	256				<-- WE STOPPED SYNCING MESA SUPPORT AT 0.11.0 SINCE THE REF DESIGN REMOVED A PULL UP AND WE NEED 1V85 ON THE LDO
T585	REF_KBD_SUPPORT	251				<-- WE STOPPED SYNCING KBD AT 0.25.0 TO FIX CREF GENERATION ERROR ON PIN Y8

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REFERENCE DESIGNS WHERE NET NUDGE WAS NEEDED TO REMOVE CREFER ERRORS
S5E, USBC, SECDIS SAK

SYNC_MASTER T668_MLB SYNC_DA E=07/17/2019

PAGE TITLE
REFERENCE DESIGN SYNC TABLES

TOP SIDE STANDOFFS

ALLOW_APPLE_PREFIX=Z
Z0400
2.80D1.2ID-1.49H-SM
CRITICAL
860-01216

ALLOW_APPLE_PREFIX=Z
Z0401
2.80D1.2ID-1.49H-SM
CRITICAL
860-01216

ALLOW_APPLE_PREFIX=Z
Z0402
2.80D1.2ID-1.49H-SM
CRITICAL
860-01216

ALLOW_APPLE_PREFIX=Z
Z0403
2.80D1.2ID-1.49H-SM
CRITICAL
860-01216

ALLOW_APPLE_PREFIX=Z
Z0404
2.80D1.2ID-1.49H-SM
CRITICAL
860-01216

ALLOW_APPLE_PREFIX=Z
Z0405
2.80D1.2ID-1.49H-SM
CRITICAL
860-01216

DFR WASHER

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0431
4.75OD2.73ID-H0.2
RING-TH
860-01519

USB-C BOSS

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0420
3.40OD1.75ID-1.12H-SM
860-00392

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0421
3.40OD1.75ID-1.12H-SM
860-00392

DFR BOSS

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0430
3.40OD1.75ID-1.5H-SM
860-01484

BOTTOM SIDE STANDOFFS

ALLOW_APPLE_PREFIX=Z
Z0410
2.80D1.2ID-3.15H-SM
CRITICAL
860-01485

ALLOW_APPLE_PREFIX=Z
Z0411
2.80D1.2ID-3.15H-SM
CRITICAL
860-01485

ALLOW_APPLE_PREFIX=Z
Z0412
2.80D1.2ID-3.15H-SM
CRITICAL
860-01485

ALLOW_APPLE_PREFIX=Z
Z0413
2.80D1.2ID-3.15H-SM
CRITICAL
860-01485

TRACKPAD BOSS

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0440
3.50D1.85ID-1.41H-SM
860-00381

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0441
3.50D1.85ID-1.41H-SM
860-00381

CPU THERM STAGE HOLE 3.15 MM

OMIT
CRITICAL
ZT0400
3P9R3P15
998-0845
CORNER NEAREST KEYBOARD

CPU THERM STAGE HOLES 3.6 MM

OMIT
CRITICAL
ZT0401
4.0R3.6-NSP
998-03850

OMIT
CRITICAL
ZT0402
4.0R3.6-NSP
998-03850

CPU THERM STAGE HOLE OVAL

OMIT
CRITICAL
ZT0403
TH-NSP
SL-3.65X3.15-4.5X4.0
ALLOW_APPLE_PREFIX=ZT
998-21974

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WIFI COAX STANDOFF

CRITICAL
Z0498
5.25X2.8R-1.4ID-1.5H-SM
ALLOW_APPLE_PREFIX=Z
860-01704

DISPLAY BOSS

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0450
2.7X1.8R-1.4ID-0.84H-SM

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0451
2.7X1.8R-1.4ID-0.84H-SM

FAN MTG HOLE 2.0X2.6 MM

OMIT
ALLOW_APPLE_PREFIX=ZT
CRITICAL
ZT0430
TH-NSP
1
SL-2.6X2.0-4.7X4.1

MLB MTG HOLES 2.1X3.51 MM

OMIT
ALLOW_APPLE_PREFIX=ZT
CRITICAL
ZT0420
TH-NSP
1
SL-2.1X3.51-4.6X6.01

OMIT
ALLOW_APPLE_PREFIX=ZT
CRITICAL
ZT0421
TH-NSP
1
SL-2.1X3.51-4.6X6.01

OMIT
ALLOW_APPLE_PREFIX=ZT
CRITICAL
ZT0422
TH-NSP
1
SL-2.1X3.51-4.6X6.01

WIFI WASHER

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0432
4.75OD2.73ID-H0.2
RING-TH

AJ FLEX COWLING BOSS

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0470
3.50D1.85ID-1.92H-SM

SHIELD CAN ALIGNMENT HOLES

OMIT
ALLOW_APPLE_PREFIX=Z
Z04A0
TH-NSP
SL-1.2X0.4-1.5X0.7
998-04440

OMIT
ALLOW_APPLE_PREFIX=Z
Z04A1
TH-NSP
SL-1.2X0.4-1.5X0.7
998-04440

OMIT
ALLOW_APPLE_PREFIX=Z
Z04A2
TH-NSP
SL-1.2X0.4-1.5X0.7
998-04440

OMIT
ALLOW_APPLE_PREFIX=Z
Z04A3
TH-NSP
SL-1.2X0.4-1.5X0.7
998-04440

OMIT
ALLOW_APPLE_PREFIX=Z
Z04A4
TH-NSP
SL-1.2X0.4-1.5X0.7
998-04440

OMIT
ALLOW_APPLE_PREFIX=Z
Z04A5
TH-NSP
SL-1.2X0.4-1.5X0.7
998-04440

POGO PINS

ALLOW_APPLE_PREFIX=PP
PP0400
POGO-2.3OD-4.0H-SM
SM-1
870-09667

ALLOW_APPLE_PREFIX=PP
PP0401
POGO-2.3OD-4.0H-SM
SM-1
870-09667

ALLOW_APPLE_PREFIX=PP
PP0402
POGO-2.3OD-4.0H-SM
SM-1
870-09667

ALLOW_APPLE_PREFIX=PP
PP0403
POGO-2.3OD-4.0H-SM
SM-1
870-09667

FENCE SPMU

PART NUMBER	DESCRIPTION	REFERENCE DES	CRITICAL	
806-24457	FENCE,SPMU,X1727	FENCE_SPMU	CRITICAL	FENCE_SPMU_C770
806-24550	FENCE,SPMU,SUS,SBP,X1727	FENCE_SPMU	CRITICAL	FENCE_SPMU_SUS

FENCE COMBO

PART NUMBER	DESCRIPTION	REFERENCE DES	CRITICAL	
806-24549	FENCE,COMBO,X1727	FENCE_COMBO	CRITICAL	FENCE_COMBO

FENCE USBC

PART NUMBER	DESCRIPTION	REFERENCE DES	CRITICAL	
806-24455	FENCE,BURNSIDE BRIDGE,X1727	FENCE_USBC	CRITICAL	FENCE_USBC_C770
806-24548	FENCE,BURNSIDE BRIDGE,SUS,SBP,X1727	FENCE_USBC	CRITICAL	FENCE_USBC_SUS

LANDING CLIP

PART NUMBER	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-25216	CLIP,LAND NG,MLB,X1727	CLIP	CRITICAL	CL P:YES

LANDING CLIP SMALL

PART NUMBER	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-25217	CLIP,LANDING,SMALL,MLB,X1727	CLIP_SMALL	CRITICAL	CLIP_SMALL:YES

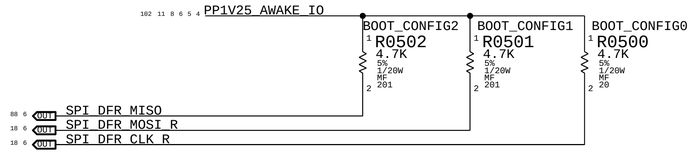
METAL SLED

PART NUMBER	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-24419	SLED,METAL,X1727	SLED1,SLED2	CRITICAL	SLED:YES

BOM_COST_GROUP=MECHANICALS

PAGE TITLE
PD PARTS

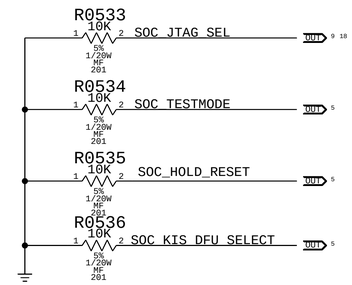
BOOT CONFIG ID



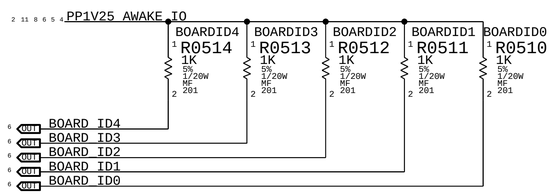
BOOT_CFG[2:0]	MODE
000	SPI1 NOR (12 MHZ)
001	SPI1 NOR (12 MHZ) TESTMODE
010	SPI0 NAND
011	SPI0 NAND TESTMODE
POR ---> 100	SPI1 NOR (40 MHZ)
101	SPI1 NOR (40 MHZ) TESTMODE
110	SPI1 NOR (6 MHZ)
111	SPI1 NOR (6MHZ) TESTMODE

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ



BOARD ID



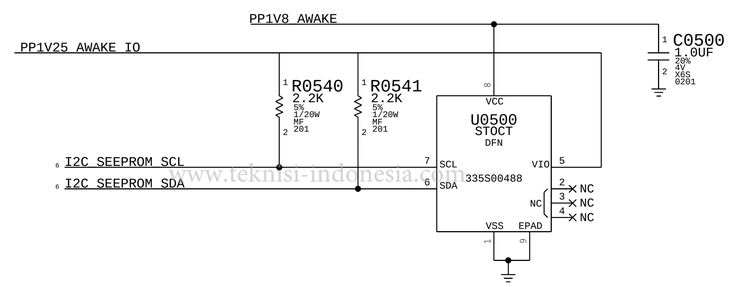
BOARD_ID[7:0] IS 8 TOTAL BITS
BOARD_ID[7:5] ARE SET INSIDE THE SOC
BOARD_ID[4:0] ARE SET WITH THESE RESISTORS
BOARD_ID[0] IS 0 FOR FORM FACTOR AND 1 FOR DEV PLATFORM
BOARD_ID[7:0] FOR J293 IS 0B00100100
<RDAR://53744986>

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

SEP EEPROM (128-Kbit)

(Write: 0xA2, Read 0xA3)
A1 PER <RDAR://590 9073>



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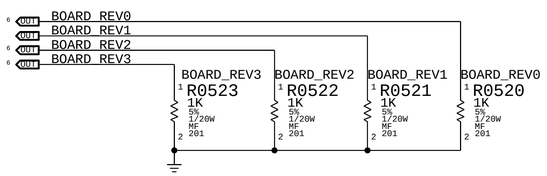
BOARD REVISION

NOTE: STUFFING RESISTOR MEANS 0



board rev should start at 0b0000 and increment each rev.

S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

J293 BOARD_REV [3:0] = 0000 : PRE P1
0001 : P1 A0
0010 : P1 A1
0011 : P1 A1 AUDIO
0100 : P2
0101 : EVT

BOM_COST_GROUP=SOC

PAGE TITLE

SOC: Support

SOC: CIO, USB, DRAM, RESETS, CLOCKS, SWD, FPWM

OMIT_TABLE

U0600
TMLR68A0-B09
BGA
SYM 1 OF 23

RESET

Signal	Pin	Block
PMU_RESET_L	R2	LP4_IN_RESET_N
SOC_FORCE_DFU	AA49	FORCE_DFU
SOC_REQUEST_DFU1	AK55	REQUEST_DFU1
SOC_REQUEST_DFU2	AJ54	REQUEST_DFU2
SOC_TESTMODE	AD	TESTMODE IPD
PMU_ACTIVE_READY	AL54	CFSB
SOC_HOLD_RESET	AC1	HOLD_RESET IPD
SOC_KIS_DFU_SELECT	AB49	KIS_DFU_SELECT
EUSB_ATC0_P	BB54	ATC0_USB_EDP
EUSB_ATC0_N	BB55	ATC0_USB_EDM
CIO_ATC0_LSRX_1V2	BE18	USB_C0_LSRX
CIO_ATC0_LSTX_1V2	BE13	USB_C0_LSTX
SOC_ATC0_USB_RESREF	BB53	ATC0_USB_RESREF
NC_ATC0_HPD	V48	USB_C0_HPD/TMU_CLK_OUT0
EUSB_ATC1_P	BC54	ATC1_USB_EDP
EUSB_ATC1_N	BC55	ATC1_USB_EDM
CIO_ATC1_LSRX_1V2	BD3	USB_C1_LSRX
CIO_ATC1_LSTX_1V2	BE10	USB_C1_LSTX
SOC_ATC1_USB_RESREF	BC53	ATC1_USB_RESREF
NC_ATC1_HPD	R48	USB_C1_HPD/TMU_CLK_OUT1
USB_VBUS_DETECT	AG1	EUSB_VBUS_DETECT
USBC_ATC0_D2R_P<1> (GND_VOID=TRUE)	BE50	ATCPHY0_RX0_P
USBC_ATC0_D2R_N<1> (GND_VOID=TRUE)	BF50	ATCPHY0_RX0_N
USBC_ATC0_R2D_C_P<1> (GND_VOID=TRUE)	BC49	ATCPHY0_TX0_P
USBC_ATC0_R2D_C_N<1> (GND_VOID=TRUE)	BD49	ATCPHY0_TX0_N
USBC_ATC0_D2R_P<2> (GND_VOID=TRUE)	BE48	ATCPHY0_RX1_P
USBC_ATC0_D2R_N<2> (GND_VOID=TRUE)	BF48	ATCPHY0_RX1_N
USBC_ATC0_R2D_C_P<2> (GND_VOID=TRUE)	BC47	ATCPHY0_TX1_P
USBC_ATC0_R2D_C_N<2> (GND_VOID=TRUE)	BD47	ATCPHY0_TX1_N
USBC_ATC0_AUX_P	AY51	ATCPHY0_AUX_P
USBC_ATC0_AUX_N	AY52	ATCPHY0_AUX_N
SOC_ATCPHY0_RCAL_POS	BE52	ATCPHY0_RCAL_P
SOC_ATCPHY0_RCAL_NEG	BF52	ATCPHY0_RCAL_N
USBC_ATC1_D2R_P<1> (GND_VOID=TRUE)	BF44	ATCPHY1_RX0_P
USBC_ATC1_D2R_N<1> (GND_VOID=TRUE)	BE44	ATCPHY1_RX0_N
USBC_ATC1_R2D_C_P<1> (GND_VOID=TRUE)	BD43	ATCPHY1_TX0_P
USBC_ATC1_R2D_C_N<1> (GND_VOID=TRUE)	BC43	ATCPHY1_TX0_N
USBC_ATC1_D2R_P<2> (GND_VOID=TRUE)	BF46	ATCPHY1_RX1_P
USBC_ATC1_D2R_N<2> (GND_VOID=TRUE)	BE46	ATCPHY1_RX1_N
USBC_ATC1_R2D_C_P<2> (GND_VOID=TRUE)	BD45	ATCPHY1_TX1_P
USBC_ATC1_R2D_C_N<2> (GND_VOID=TRUE)	BC45	ATCPHY1_TX1_N
USBC_ATC1_AUX_P	BA52	ATCPHY1_AUX_P
USBC_ATC1_AUX_N	BA51	ATCPHY1_AUX_N
SOC_ATCPHY1_RCAL_POS	BF4	ATCPHY1_RCAL_P
SOC_ATCPHY1_RCAL_NEG	BE4	ATCPHY1_RCAL_N

ATC

Signal	Pin	Block
DFU_STATUS	V51	SOC_DFU_STATUS
XI0	BE36	SOC_XTAL24M_IN
XO0	BF36	SOC_XTAL24M_OUT
TST_CLKOUT	P54	TP_TST_CLKOUT
ANALOGMUX_OUT	AL48	TP_SOC_AMUX_OUT
SWD_TCK_OUT1	AJ1	SWD_NAND0_SWCLK
SWD_TMS2	U54	SWD_NAND0_SWDIO
SWD_TMS3	V54	NC_SWD_TMS3
SWD_TMS4	AH3	TP_SWD_TMS4
FPWM0/MASTER_SYNC_GEN_0	V50	IPD WLAN_TIME_SYNC
FPWM1	Y49	KBD_BKLT_PWM
FPWM2	U50	TP_FPWM2

CLOCKS

SWD

FPW

AMUX_OUT can go to TP or to AMUX_IN on PMU

R0651 99 1% 1/20W MF 201

CRITICAL Y0600 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM OC 24M O R

CRITICAL C0650 15PF 5% 50V C0G 0201

CRITICAL C0651 15PF 5% 50V C0G 0201

SOC_ATCPHY0_RCAL_POS — R0600 200 1% 1/20W MF 201

SOC_ATCPHY0_RCAL_EG — C0600 10PF 5% 25V C0G 0201

SOC_ATCPHY1_RCAL_POS — R0601 200 1% 1/20W MF 201

SOC_ATCPHY1_RCAL_NEG — C0601 10PF 5% 25V C0G 0201

PP1V25_AWAKE_IO — R0630 10K 5% 1/20W MF 201 — SOC_REQUEST_DFU1

PP1V25_AWAKE_IO — R0631 10K 5% 1/20W MF 201 — SOC_REQUEST_DFU2

SOC_FORCE_DFU — R0632 47K 5% 1/20W MF 201

SOC_ATC0_USB_RESREF — R0641 200 1% 1/20W MF 201

SOC_ATC1_USB_RESREF — R0640 200 1% 1/20W MF 201

PP1V25_AWAKE_IO — R0639 0 5% 1/20W MF 0201 — USB_VBUS_DETECT

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0590	197S0591		Y0600	EPSON,24MHZ.XTAL
197S0588	197S0591		Y0600	TXC,24MHZ,XTAL

BOM_COST_GROUP=SOC

SYNC_MASTER=HATHEN_T8_8_MLB SYNC_DATE=10/08/2010

PAGE TITLE

SOC: CIO, USB, RESETS, CLOCKS, SWD

A

6 5 4 3

OK2INTEGRATE

all signals are 1.2 unless otherwise specified.
all signals on this page reference PP1V2_AWAKE_GRP if they are 1.2V
if they are 1.8V they reference PP1V8_AWAKE_GRP

SOC: I/Os

U0600 TMLR68A0-B09 BGA SYM 3 OF 23

Signal	Pin	Dir	Net
I2S0_BCLK	AK4	OUT	TDM_SPKRAMP_L_BCLK_R
I2S0_DIN (IPD)	AJ3	IN	TDM_SPKRAMP_L_D2R
I2S0_DOUT	AJ5	OUT	TDM_SPKRAMP_L_R2D_R
I2S0_LRCK	AJ4	OUT	TDM_SPKRAMP_L_FSYNC_R
I2S0_MCK	AK3		NC_SOC_I2S0_MCK
I2S1_BCLK	AG3	OUT	TDM_SPKRAMP_R_BCLK_R
I2S1_DIN (IPD)	AF3	IN	TDM_SPKRAMP_R_D2R
I2S1_DOUT	AG4	OUT	TDM_SPKRAMP_R_R2D_R
I2S1_LRCK	AF2	OUT	TDM_SPKRAMP_R_FSYNC_R
I2S1_MCK	AG2		NC_SOC_I2S1_MCK
I2S2_BCLK	AK5	OUT	TDM_CODEC_BCLK_R
I2S2_DIN (IPD)	AL6	IN	TDM_CODEC_D2R
I2S2_DOUT	AJ7	OUT	TDM_CODEC_R2D_R
I2S2_LRCK	AM4	OUT	TDM_CODEC_FSYNC_R
I2S2_MCK	AK6		TP_SOC_I2S2_MCK
I2S3_BCLK	AH6		NC_I2S3_BCLK
I2S3_DIN	AH4		NC_I2S3_D2R
I2S3_DOUT	AG5		NC_I2S3_R2D
I2S3_LRCK	AJ6		NC_I2S3_LRCLK
I2S3_MCK	AF5		NC_I2S3_MCLK
I2C0_SCL	W52	OUT	I2C_UPC_SCL
I2C0_SDA	V52	BI	I2C_UPC_SDA
I2C1_SCL	AA48	OUT	I2C_SPKRAMP_L_SCL
I2C1_SDA	Y48	BI	I2C_SPKRAMP_L_SDA
I2C2_SCL	AB50	OUT	I2C_CODEC_SCL
I2C2_SDA	Y50	BI	I2C_CODEC_SDA
I2C3_SCL	AF6	OUT	I2C_SPKRAMP_R_SCL
I2C3_SDA	AE6	BI	I2C_SPKRAMP_R_SDA
I2C4_SCL	AF50	OUT	I2C_DFR_SCL
I2C4_SDA	AG49	BI	I2C_DFR_SDA
AP_SPMI2_SCLK	AK7		NC_SPMI2_CLK
AP_SPMI2_SDATA	AL7		TP_SPMI2_DATA

1.8V IO

Signal	Pin	Dir	Net
SPI0_MISO (IPD)	AL4	IN	SPI_DFR_MISO
SPI0_MOSI	AK2	OUT	SPI_DFR_MOSI_R
SPI0_SCLK	AK1	OUT	SPI_DFR_CLK_R
SPI1_MISO (IPD)	AD4	IN	SPI_SOCROM_MISO
SPI1_MOSI	AE4	OUT	SPI_SOCROM_MOSI_R
SPI1_SCLK	AF4	OUT	SPI_SOCROM_CLK_R
SPI1_SSIN	AE3	OUT	SPI_SOCROM_CS_L
SPI2_MISO (IPD)	AF53	IN	SPI_TOUCHID_MISO
SPI2_MOSI	AF54	OUT	SPI_TOUCHID_MOSI_R
SPI2_SCLK	AF55	OUT	SPI_TOUCHID_CLK_R
SPI2_SSIN	AF52		NC_SOC_SPI2_SSIN
SPI3_MISO (IPD)	Y1	IN	SPI_IPD_MISO
SPI3_MOSI	W1	OUT	SPI_IPD_MOSI_R
SPI3_SCLK	AB1	OUT	SPI_IPD_CLK_R
SPI3_SSIN	AA1	OUT	SPI_IPD_CS_L
SPI4_MISO (IPD)	AC4	IN	SPI_TCON_MISO
SPI4_MOSI	AB4	OUT	SPI_TCON_MOSI_R
SPI4_SCLK	AA4	OUT	SPI_TCON_CLK_R
SPI4_SSIN	AB3	OUT	SPI_TCON_CS_L
SGPIO0	AC3	IN	DBL_CLICK_DET
SGPIO1	AC2	OUT	DISABLE_STROBE
SI2C0_SCL	Y5	OUT	I2C_SEEPROM_SCL
SI2C0_SDA	Y4	BI	I2C_SEEPROM_SDA
SSPI0_MISO	AC5	OUT	FTCAM_DISABLE_L
SSPI0_MOSI	AD5		NC_SSPI0_MOSI
SSPI0_SCLK	AD6	OUT	DMIC_DISABLE_L
SOCHOT1	AK52	OUT	SOC_SOCHOT_L
THROTTLE_TRIGGER0/MTR_ADC_DOUT	AK53	IN	BUCK1_THERMAL_THROTTLE_L
THROTTLE_TRIGGER1/MTR_ADC_CLKOUT	AL53	IN	BUCK0_THERMAL_THROTTLE_L
THROTTLE_TRIGGER2/PLL_DIGOBS_0	AJ55	IN	SOC_THROTTLE_TRIGGER2
THROTTLE_TRIGGER3/PLL_DIGOBS_1	AJ53	IN	PMU_VDDHI_UVWARN_L
THROTTLE_TRIGGER4	AJ49	IN	PMU_VDDMAIN_UVWARN_L

THROTTLE — IPU FOR ALL THROTTLE_TRIGGER

1.8V IO

PP1V25_AWAKE_IO — R0790 47K 5% 1/20W MF 201 — SOC_SOCHOT_L

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U0600 TMLR68A0-B09 BGA SYM 2 OF 23

UPC_FORCE_PWR will likely be removed in the future

TOUCHID_PWR_EN gets pulled up to S2 on TOUCHID page This is OK because the GPIO is failsafe

PD needed on DFR PAGE

Signal	Pin	Dir	Net
GPIO[0] (IPU)	AJ51	IN	UPC_I2C_INT_L
GPIO[1]	AA50		NC_SOC_GPIO01
GPIO[2] (IPU)	V53	IN	SPKR_ID0
GPIO[3] (IPU)	U53	IN	SPKR_ID1
GPIO[4]	T53	OUT	SPKRAMP_RESET_L
GPIO[5] (IPU)	W53	IN	SPKRAMP_INT_L
GPIO[6] (IPU)	W50	IN	CODEC_INT_L
GPIO[7]	U52	OUT	SWD_UPC_SWCLK
GPIO[8]	AC48		NC_SOC_GPIO08
GPIO[9]	R53		TP_SOC_GPIO09
GPIO[10]	R52		TP_SOC_GPIO10
GPIO[11]	N55	IN	BOARD_REV0
GPIO[12]	AH54	IN	BOARD_REV1
GPIO[13]	Y52	IN	BOARD_REV2
GPIO[14]	AA51	IN	BOARD_REV3
GPIO[15]	R54		NC_SOC_GPIO15
GPIO[16]	AC50		NC_SOC_GPIO16
GPIO[17]	U51	BI	SWD_UPC_SWDIO0
GPIO[18]	AK50	BI	TP_SWD_UPC_SWDIO1
GPIO[19]	T52	IN	DFR_TOUCH_INT_L
GPIO[20]	V49	OUT	IPD_SPI_EN
GPIO[21] (IPD)	AJ52	IN	TOUCHID_INT
GPIO[22]	AJ50	OUT	TOUCHID_PWR_EN
GPIO[23]	AC49	OUT	UPC_FORCE_PWR
GPIO[24]	R51	OUT	DFR_PWR_EN
GPIO[25]	AL49	OUT	SPI_DFR_CS_L
GPIO[26] (IPD)	AF49	IN	NC_ENET_SYNC_1588
BOARD_ID0/SOC_DEBUG1	W49	IN	BOARD_ID0
BOARD_ID1/SOC_DEBUG2	R55	IN	BOARD_ID1
BOARD_ID2/SOC_DEBUG3	T55	IN	BOARD_ID2
BOARD_ID3/SPI0_SSIN	V55	IN	BOARD_ID3
BOARD_ID4	U55	IN	BOARD_ID4

1.8V IO

Signal	Pin	Dir	Net
UART0_RXD (IPD)	AB53	IN	UART_DEBUGPRT_D2R
UART0_TXD	AC53	OUT	UART_DEBUGPRT_R2D
UART1_CTSN	AC54	OUT	DFR_1V8_TOUCH_RESET_L
UART1_RTSN	AA53	OUT	DFR_1V8_DISP_RESET_L
UART1_RXD (IPD)	AA54	IN	DFR_1V8_DISP_INT
UART1_TXD (IPD)	AC55	IN	BT_TIME_SYNC_1V8
UART2_CTSN (IPU)	W55	IN	UART_WLAN_D2R_CTS_L
UART2_RTSN	Y54	OUT	UART_WLAN_R2D_RTS_L
UART2_RXD (IPU)	Y53	IN	UART_WLAN_D2R
UART2_TXD	Y55	OUT	UART_WLAN_R2D
UART3_CTSN	AC51		NC_UART3_D2R_CTS_L
UART3_RTSN	AC52		NC_UART3_R2D_RTS_L
UART3_RXD	AF48		NC_UART3_D2R
UART3_TXD	AB52		NC_UART3_R2D
UART4_CTSN	AJ48		NC_UART4_D2R_CTS_L
UART4_RTSN	AK48		NC_UART4_R2D_RTS_L
UART4_RXD	AL52		NC_UART4_D2R
UART4_TXD	AL50		NC_UART4_R2D
UART6_RXD	AF51	IN	UART_TCON_HDMI_D2R
UART6_TXD	AG50	OUT	UART_TCON_HDMI_R2D
UART7_RXD	AM2		NC_UART7_RXD
UART7_TXD	AJ2		NC_UART7_TXD
NAND_SYS_CLK0	AG52	OUT	NAND0_CLK24M_0_R
NAND_SYS_CLK1	AH53	OUT	NAND0_CLK24M_1_R
SSD_BFH	AH51	OUT	NAND_BFH
SSD_RESETN	AG53	OUT	NAND0_RESET_L

1.8V IO

s UART2 if your wireless module is 1.2V IO

1.8V IO R2D is for desktop only

NAND0_RESET_L — NOSTUFF R0791 47K 5% 1/20W MF 201

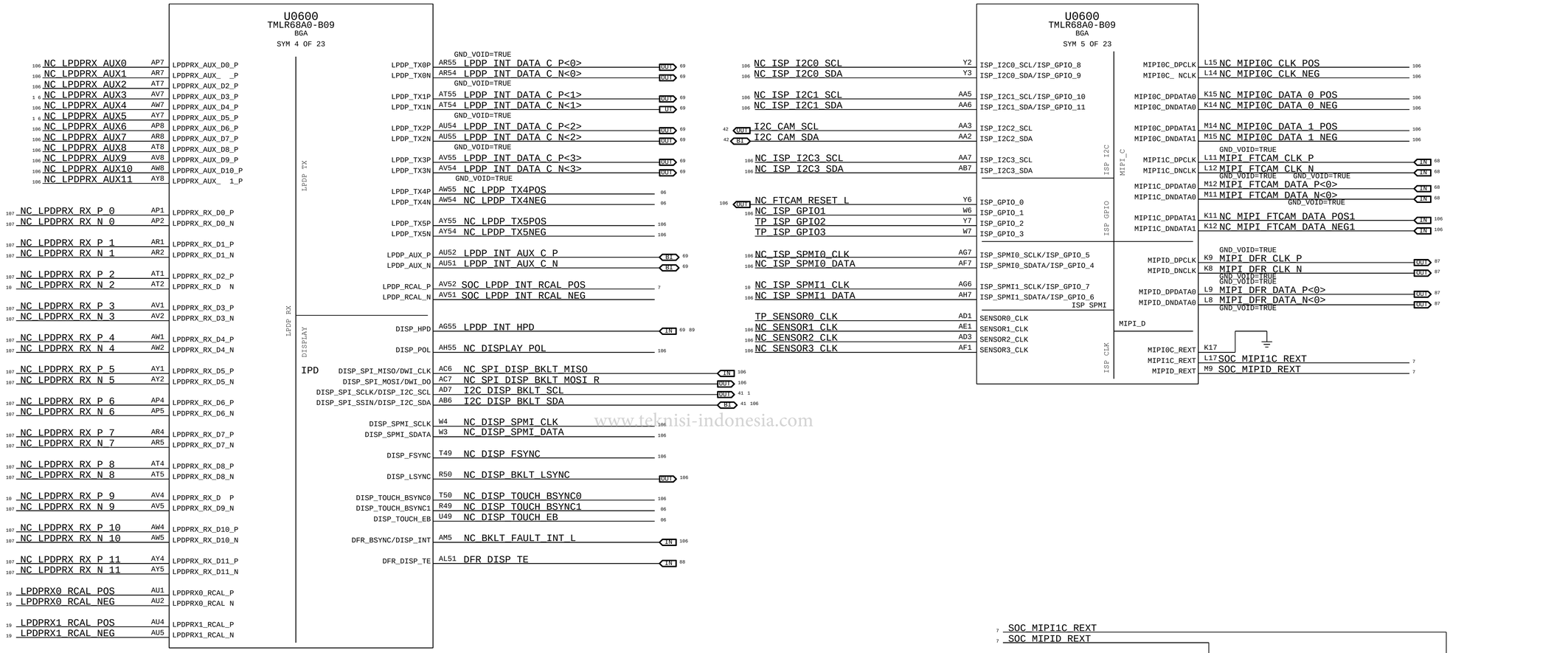
BOM_COST_GROUP=SOC

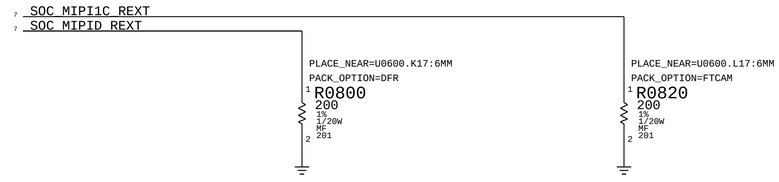
PAGE TITLE

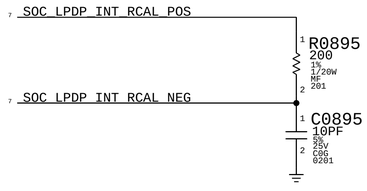
SOC: AP I/Os

OK2INTEGRATE

SOC: LPDP & MIPI







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SYNC_MASTER=AITKEN_T668_MLB SYNC_DATE=10/08/2010

PAGE TITLE

SOC: LPDP & MIPI

BOM_COST_GROUP=SOC

SOC: PCIE

PER PCISIG SPEC, AC COUPLING CAPS SHOULD BE BETWEEN
75 NF AND 265 NF FOR GEN1/2 AND BETWEEN
176 NF AND 265 NF FOR GEN 3/4

R0970 IS NEEDED DUE TO RDAR://53793006

102 11 6 5 4 PP1V25_AWAKE_IO

R0930 47K 5% 1/20W MF 201
R0940 47K 5% 1/20W MF 201
R0950 47K 5% 1/20W MF 201
R0970 47K 5% 1/20W MF 201

67 8 NAND0_CLKREQ1_L
63 62 8 WLBT_CLKREQ_L
67 8 NAND0_CLKREQ0_L
8 USBHC_CLKREQ_L

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TMLR68A0-B09
BGA
SYM 6 OF 23

NAND

64 IN	PCIE_NAND0_D2R_P<0>	BE26	ST_PCIE_RX0_P	GP_PCIE_RX0_P	BE30	PCIE_WLBT_D2R_P	IN 62
64 IN	PCIE_NAND0_D2R_N<0>	BF26	ST_PCIE_RX0_N	GP_PCIE_RX0_N	BF30	PCIE_WLBT_D2R_N	IN 62
64 OUT	PCIE_NAND0_R2D_C_P<0>	BC27	ST_PCIE_TX0_P	GP_PC E_TX0_P	BC31	PCIE_WLBT_R2D_C_P	OUT 62
64 OUT	PCIE_NAND0_R2D_C_N<0>	BD27	ST_PCIE_TX0_N	GP_PCIE_ X0_N	BD31	PCIE_WLBT_R2D_C_N	OUT 62
67 64 OUT	PCIE_CLK100M_NAND0_0_P	BB37	ST_PCIE_REF_CLK0_P	GP_PCIE_REF_CLK0_P	BE40	PCIE_CLK100M_WLBT_P	OUT 62
67 64 OUT	PCIE_CLK100M_NAND0_0_N	BC37	ST_PCIE_REF_CLK0_N	GP_PCIE_REF_CLK0_N	BF40	PCIE_CLK100M_WLBT_N	OUT 62
67 8 BI	NAND0_CLKREQ0_L	AH50	ST_PCIE_CLKREQ0_N	GP_PCIE_CLKREQ0_N	AB55	WLBT_CLKREQ_L	BI 8 62 63
67 64 8 65 OUT	NAND0_PCIE_RESET_L	AH52	ST_PCIE_PERST0_N	GP_PCIE_PERST0_N	AA52	WLBT_RESET_L	OUT 8 62 63

WLAN/BT

65 IN	PCIE_NAND0_D2R_P<1>	BE28	ST_PCIE_RX1_P	GP_PCIE_RX1_P	BE32	NC_PCIE_USBHC_D2R_POS	IN 1 6
65 IN	PCIE_NAND0_D2R_N<1>	BF28	ST_PCIE_RX1_N	GP_PCIE_RX1_N	BF32	NC_PCIE_USBHC_D2R_NEG	IN 106
65 OUT	PCIE_NAND0_R2D_C_P<1>	BC29	ST_PCIE_TX1_P	GP_PCIE_TX1_P	BC33	NC_PCIE_USBHC_R2D_C_POS	OUT 106
65 OUT	PCIE_NAND0_R2D_C_N<1>	BD29	ST_PCIE_TX1_N	GP_PCIE_TX1_N	BD33	NC_PCIE_USBHC_R2D_C_NEG	OUT 106
67 65 OUT	PCIE_CLK100M_NAND0_1_P	BB38	ST_PCIE_REF_CLK1_P	GP_PCIE_REF_CLK1_P	BE38	NC_PCIE_CLK100M_USBHC_POS	OUT 106
67 65 OUT	PCIE_CLK100M_NAND0_1_N	BC38	ST_PCIE_REF_CLK1_N	GP_PCIE_REF_CLK1_N	BF38	NC_PCIE_CLK100M_USBHC_NEG	OUT 106
67 8 BI	NAND0_CLKREQ1_L	AH49	ST_PCIE_CLKREQ1_N	GP_PCIE_CLKREQ1_N	AA55	USBHC_CLKREQ_L	8
106	NC_NAND0_PCIE_RESET1_L	AH48	ST_PCIE_PERST1_N	GP_PCIE_PERST1_N	P55	NC_USBHC_RESET_L	OUT 106

USB3 CTLR

				GP_PCIE_RX2_P	BE34	NC_PCIE_ENET_D2R_POS	IN 106
				GP_PCIE_RX2_N	BF34	NC_PCIE_ENET_D2R_NEG	IN 106
				GP_PCIE_TX2_P	BC35	NC_PCIE_ENET_R2D_C_POS	OUT 106
				GP_PCIE_TX2_N	BD35	NC_PCIE_ENET_R2D_C_NEG	OUT 106
				GP_PCIE_REF_CLK2_P	BE39	NC_PCIE_CLK100M_ENET_POS	OUT 106
				GP_PCIE_REF_CLK2_N	BF39	NC_PCIE_CLK100M_ENET_NEG	OUT 106
				GP_PCIE_CLKREQ2_N	AH1	NC_ENET_CLKREQ_L	BI 106
				GP_PCIE_PERST2_N	AE7	NC_ENET_RESET_L	OUT 106

ENET/SD

8	SOC_ST_PCIE_RCAL_POS	BC24	ST_PCIE_RCAL_P	GP_PCIE_RCAL_P	BC25	SOC_GP_PCIE_RCAL_POS	8
8	SOC_ST_PCIE_RCAL_NEG	BB24	ST_PCIE_RCAL_N	GP_PCIE_RCAL_N	BB25	SOC_GP_PCIE_RCAL_NEG	8
106	NC_MTR_VREF_ANAP	AM3	PAD_MTR_ANALOG_TEST_P				
106	NC_MTR_VREF_ANAN	AL3	PAD_MTR_ANALOG_TEST_N				
106	NC_MTR_VREF_POS	AL1	PAD_MTR_VREF_P				
106	NC_MTR_VREF_NEG	AM1	PAD_MTR_VREF_N				

PCIE GP0 | PCIE GP1 | PCIE | MT

TO BE CHECKED WITH SEG- DO NOT MATCH WITH SILVAL
IS THE PULL-UP VOLTAGE CORRECT?

8 SOC_ST_PCIE_RCAL_POS
8 SOC_ST_PCIE_RCAL_NEG

R0990 200 1% 1/20W MF 201
C0990 10PF 5% 25V C0G 0201

8 SOC_GP_PCIE_RCAL_POS
8 SOC_GP_PCIE_RCAL_NEG

R0991 200 1% 1/20W MF 201
C0991 10PF 5% 25V C0G 0201

67 65 64 8 NAND0_PCIE_RESET_L
63 62 8 WLBT_RESET_L

R0941 47K 5% 1/20W MF 201
R0951 47K 5% 1/20W MF 201

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BOM_COST_GROUP=SOC

SYNC_MASTER=ANDREW_T668_MLB SYNC_DATE=10/09/2010
PAGE TITLE
SOC: PCIE

OK2INTEGRATE

AOP, NUB, AND SMC GPIO'S ARE REFERENCED TO PP1V25_S2_AOP

SOC: AOP

U0600
TMLR68A0-B09
BGA
SYM 7 OF 23

Signal	Ball	Pin	Dir	Pull	Group
NC_R1_DUMP_TRIG	BB18	AOP_FUNC[0]	OUT		AOP GPIO
NC_AOP_FUNC1	BC16	AOP_FUNC[1]			
NC_R1_RTC_SYNC	BC12	AOP_FUNC[2]	OUT		
NC_R1_INT	BC13	AOP_FUNC[3]	IN	IPD	
NC_SPI_R1_CS_L	BA16	AOP_FUNC[4]	OUT		
NC_AOP_FUNC5	BA13	AOP_FUNC[5]			
SPI_GYRO_CS_L	BA15	AOP_FUNC[6]	OUT		
GYRO_INT	BD13	AOP_FUNC[7]	IN		
GYRO_MOTION_INT	BD16	AOP_FUNC[8]	IN		
LID_OPEN	BA14	AOP_FUNC[9]	IN	IPD	
NC_AOP_FUNC10	BB12	AOP_FUNC[10]			
WLAN_CONTEXT_A	BD20	AOP_FUNC[11]	OUT		
WLAN_CONTEXT_B	BA11	AOP_FUNC[12]	OUT		
NC_ALS_INT_L	BD18	AOP_FUNC[13]	IN	IPU	
NC_AOP_FUNC14	BA10	AOP_FUNC[14]			
I2C_AOP_ALS_SCL	BC20	AOP_I2CM0_SCL	OUT		AOP I2C
I2C_AOP_ALS_SDA	BB19	AOP_I2CM0_SDA	B		
NC_I2C_AOP_ENET_SCL	BB16	AOP_I2CM1_SCL	OUT		
NC_I2C_AOP_ENET_SDA	BE15	AOP_I2CM1_SDA	B		
NC_PDM_CLK1	BB9	AOP_PDM_IN_CLK1/AOP_I2S1_BCLK			AOP PDM
NC_PDM_CLK2	BC9	AOP_PDM_IN_CLK2/AOP_I2S0_MCK			
PDM_DMIC_CLK3	BC6	AOP_PDM_IN_CLK3/AOP_I2S0_LRCK	OUT		
PDM_DMIC_CLK4	BD9	AOP_PDM_IN_CLK4/AOP_I2S0_DOUT	OUT		
NC_PDM_CLK5	BC8	AOP_PDM_IN_CLK5/AOP_I2S0_DIN			
NC_PDM_CLK6	BD8	AOP_PDM_IN_CLK6/AOP_I2S0_BCLK			
NC_PDM_DATA1	BE21	AOP_PDM_IN_DATA1/AOP_I2S1_MCK			
NC_PDM_DATA2	BE16	AOP_PDM_IN_DATA2/AOP_I2S1_LRCK			
PDM_DMIC_DATA3 (CKP_S_W_IVE=CLK_DATA_CON)	BE19	AOP_PDM_IN_DATA3/AOP_I2S1_DOUT/AOP_PDM_IN_CLK7	IN	IPD	
PDM_DMIC_DATA4 (CKPLUS_WAIVE=CLK_DATA_CON)	BD5	AOP_PDM_IN_DATA4/AOP_I2S1_DIN/AOP_PDM_IN_CLK8	IN	IPD	
SPI_AOP_GYRO_R1_MISO	BF15	AOP_SPI0_MISO	IN		AOP SPI
SPI_AOP_GYRO_R1_MOSI_R	BF14	AOP_SPI0_MOSI	OUT		
SPI_AOP_GYRO_R1_CLK_R	BF17	AOP_SPI0_SCLK	OUT		
NC_AOP_SPMI0_SCLK	BF18	AOP_SPMI0_SCLK/AOP_UART0_TXD			AOP SPMI
NC_AOP_SPMI0_SDATA	BF19	AOP_SPMI0_SDATA/AOP_UART0_RXD			
SPMI_SE_CLK_R	BF20	AOP_SPMI1_SCLK/AOP_UART1_TXD	OUT		
SPMI_SE_DATA_R	BF21	AOP_SPMI1_SDATA/AOP_UART1_RXD	B		
NC_AOP_UART2_D2R	BB3	AOP_UART2_RXD			AOP UART
NC_AOP_UART2_R2D	BB4	AOP_UART2_TXD			
PP1V25_S2					
PMU_CLK32K_SOC	BE6	RT_CLK32768	IN		AOP RESET
	BF10	CFSB_AON			
PMU_RESET_L	BB5	COLD_RESETN	IN		
TP_AON_SLEEP1_RESET_L	BB21	AON_SLEEP1_RESETN			
SOC_WDOG	BF12	WDOG	OUT		
SOC_DBG_PROBE_VALID	BF6	DBG_PROBE_VALID			AOP DEBUG
EUSB_DBG_P	BF24	DBG_USB_EDP	B		
EUSB_DBG_N	BE24	DBG_USB_EDM	B		
SOC_USBDBG_RESREF	BE23	DBG_USB_RESREF			

Signal	Ball	Pin	Dir	Pull	Group
DFR_TOUCH_CLK32K_RESET_L	BA17	NUB_CLK_OUT0	OUT		NUB GPIO
TP_SOC_DOCK_ATTENTION	BC15	NUB_DOCK_ATTENTION/CTM_TRIGGER	B		
SOC_DOCK_CONNECT	BC17	NUB_DOCK_CONNECT	IN		
NC_BKLT_PWR_ON_SMC_LED_SEL	BD14	NUB_GPIO_0/AOP_FUNC15/NUB_CLK_OUT1	OUT		
CODEC_RESET_L	BD15	NUB_GPIO_1/AOP_PDM_IN_CLK6	OUT		
SOC_SW_DBG	BD21	NUB_GPIO_2/AOP_PDM_IN_DATA6	OUT		
IPD_SPI_INT_L	BD17	NUB_GPIO_3/AOP LEAP_MADI_IN	IN	IPU	
SMC_FIXTURE_MODE_L	BB13	NUB_GPIO_4/AOP_LEAP_MADI_OUT	IN		
CHGR_INT_L	BD19	NUB_GPIO_5/AOP_PDM_OUT_CLK6	IN		
NC_ENET_I2C_LOM_INT_L	BD22	NUB_GPIO_6/AOP_PDM_OUT_DATA0/AOP_FUNC16	IN		
NC_ACDC_ID	BB10	NUB_GPIO_7/A P_ U C17	IN		
NC_ACDC_BURST_EN_L	BD12	NUB_GPIO_8/AOP_FUNC18	OUT		
NC_SPI_DP2HDMI_HOLD_L	BD11	NUB_GPIO_9/AOP_FUNC19	OUT		
NC_HDMI_CEC_AOP_TX	BC10	NUB_GPIO_10/AOP_FUNC20	OUT		
NC_HDMI_CEC_AOP_RX	BB7	NUB_GPIO_11/KIS_GPIO0/AOP_FUNC21	IN		
NC_HDMI_HPD_AOP	BD10	NUB_GPIO_12/KIS_GPIO1/AOP_FUNC22	IN		
SPMI_NUB_MPMU_CLK_R	BB15	NUB_SPMI0_SCLK	OUT		NUB SPMI
SPMI_NUB_MPMU_DATA_R	BC14	NUB_SPMI0_SDATA	B		
SPMI_NUB_SPMU_CLK_R	BA12	NUB_SPMI1_SCLK	OUT		
SPMI_NUB_SPMU_DATA_R	BC11	NUB_SPMI1_SDATA	B		
SWD_NUB_SWCLK	BC18	NUB_SWD_TCK_OUT0	OUT		NUB SWD
SWD_NUB_PMU_SWDIO	BC19	NUB_SWD_TMS0	B		
NC_SWD_NUB_R1_SWDIO	BC21	NUB_SWD_TMS1	B		
SOC_JTAG_SEL	BE4	JTAG_SEL	IN		JTAG
SWD_SOC_SWCLK	BF5	JTAG_TCK	IN	IPU	
TP_JTAG_SOC_TDI	BF16	JTAG_TDI		IPU	
TP_JTAG_SOC_TDO	BC1	JTAG_TDO			
SWD_SOC_SWDIO	BB1	JTAG_TMS	B	IPU	
TP_JTAG_SOC_TRST_L	BF7	JTAG_TRSTN		IPD	
I2C_SMC_PWR_SCL	BC3	SMC_I2CM0_SCL	O		SMC I2C
I2C_SMC_PWR_SDA	BC2	SMC_I2CM0_SDA	B		
I2C_SMC_UPC_SCL	BD4	SMC_I2CM1_SCL/SMC_UART1_TXD	OUT		
I2C_SMC_UPC_SDA	BB2	SMC_I2CM1_SDA/SMC_UART1_RXD	B		
I2C_SMC_SNS1_SCL	BD6	SMC_I2CM2_SCL	OUT		
I2C_SMC_SNS1_SDA	BC5	SMC_I2CM2_SDA	B		
I2C_SMC_IPD_SCL	BC7	SMC_I2CM3_SCL	OUT		
I2C_SMC_IPD_SDA	BD7	SMC_I2CM3_SDA	B		
I2C_SMC_SNS0_SCL	BE7	SMC_I2CM4_SCL	OUT		
I2C_SMC_SNS0_SDA	BF9	SMC_I2CM4_SDA	B		
UART_SMC_DEBUGPRT_D2R	BF4	SMC_UART0_RXD	IN	IPU	SMC UART
UART_SMC_DEBUGPRT_R2D	BF8	SMC_UART0_TXD	OUT		
UPC_SMC_I2C_INT_L	BF11	SMC_GPIO0	IN	IPU	SMC GPIO
NC_SMC_GPIO1	BF13	SMC_GPIO1			
SMC_FAN_PWM	BE12	SMC_FPWM0	OUT		
SMC_FAN_TACH	BE9	SMC_FPWM1	IN		

DOC_ATTENTION should be a TP
for non dev programs,

SOC_SW_DBG SHOULD GO TO
A LED IF POSSIBLE.
NEEDS A TEST POINT AT MINIMUM

FIXTURE_MODE_L should be aliased to a TP
for non dev programs,
The TP is required

output if gyro, input for radar

I2C0 is ALS for portables

R1083 10K 5% 1/20W MF 201

XW1022 SHORT-14L-0.1MM SM

R1042 200 1% 1/20W MF 1

SOC_DOCK_CONNECT

R1066 47K 5% 1/20W MF 201

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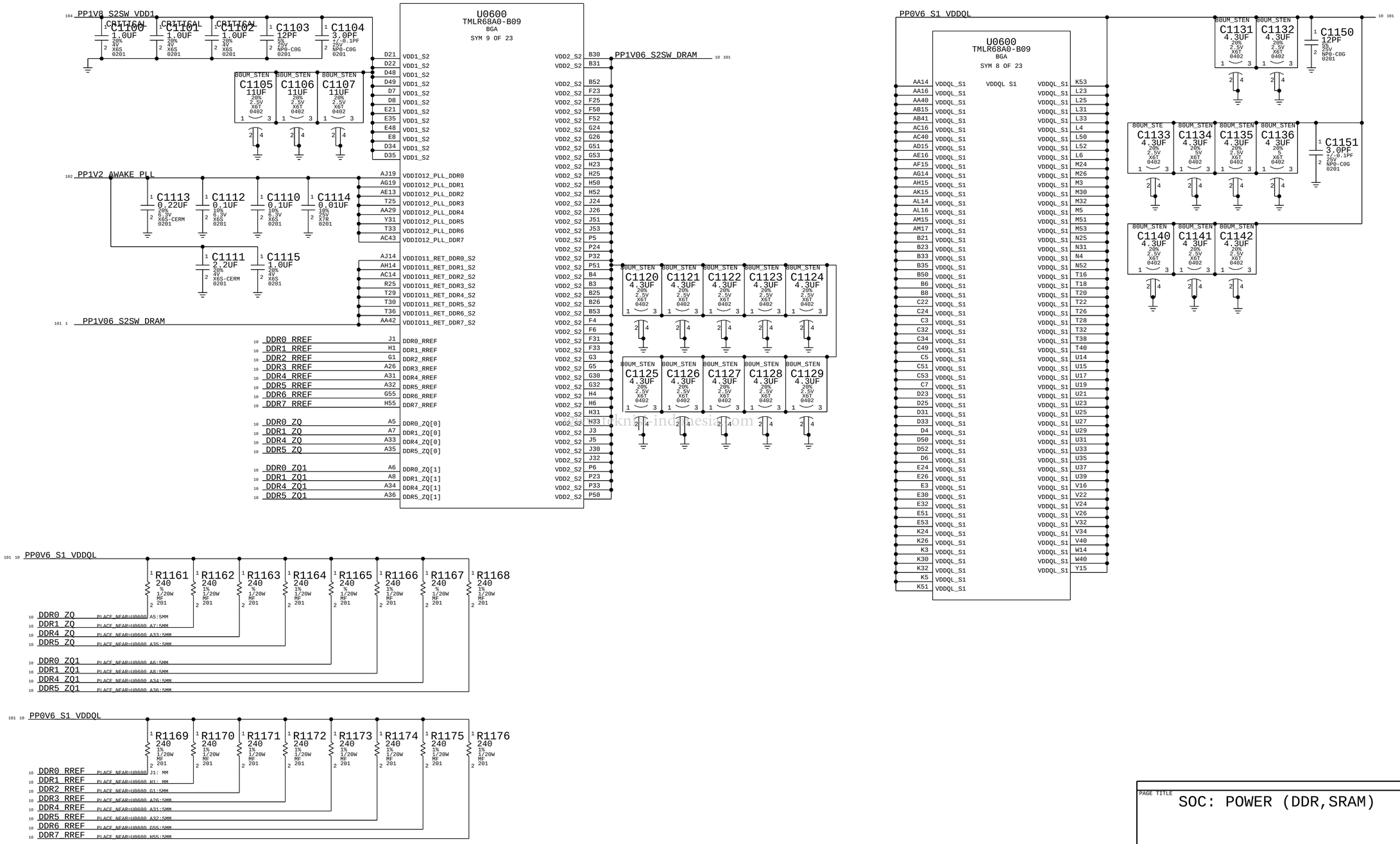
PAGE TITLE
SOC: AOP

BOM_COST_GROUP=SOC

OK2INTEGRATE

SOC: POWER (DDR,SRAM)



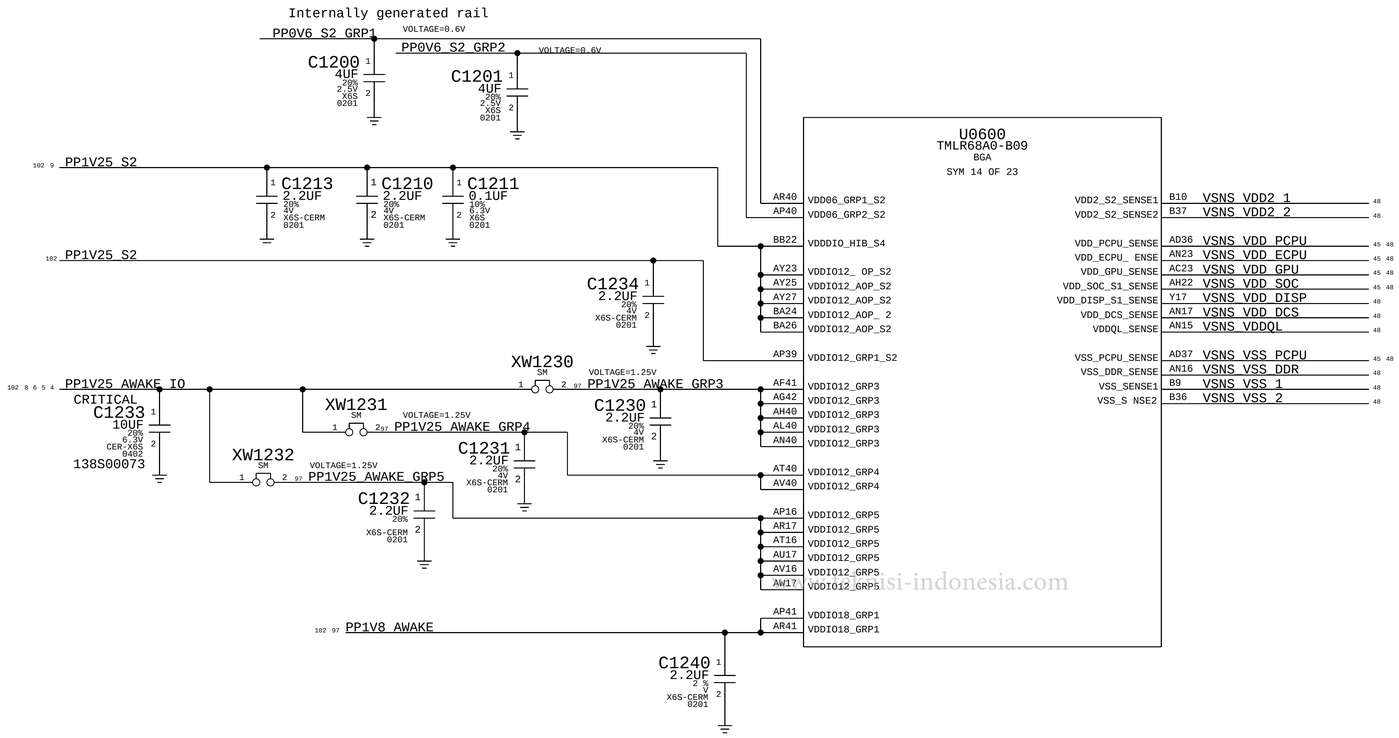
BOM_COST_GROUP=SOC

PAGE TITLE

SOC: POWER (DDR,SRAM)

OK2INTEGRATE

SOC: POWER (IO)



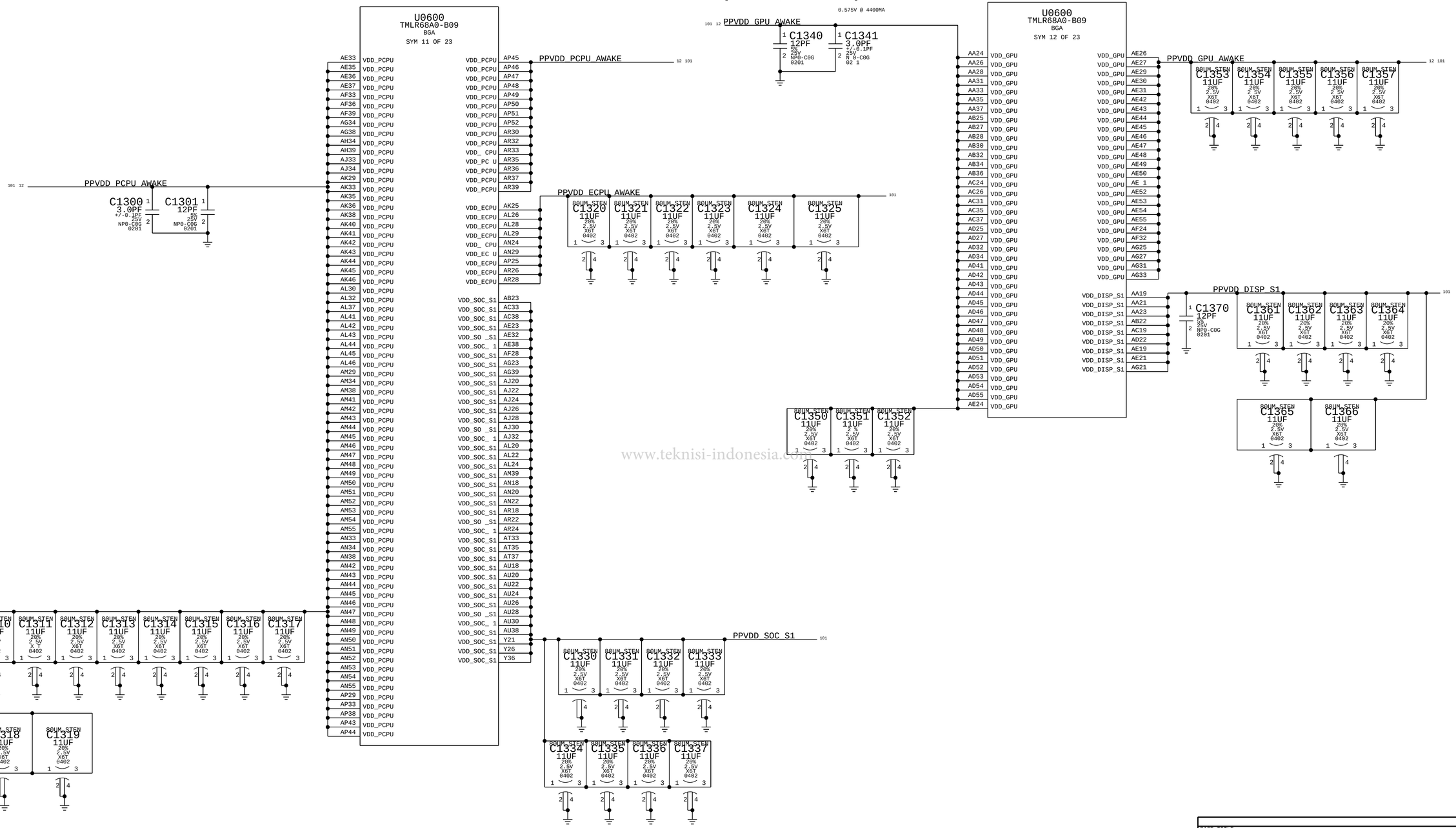
isi-indonesia.com

SOC: POWER (IO)

BOM_COST_GROUP=SOC

OK2INTEGRATE

SOC: POWER (CPU, GPU)



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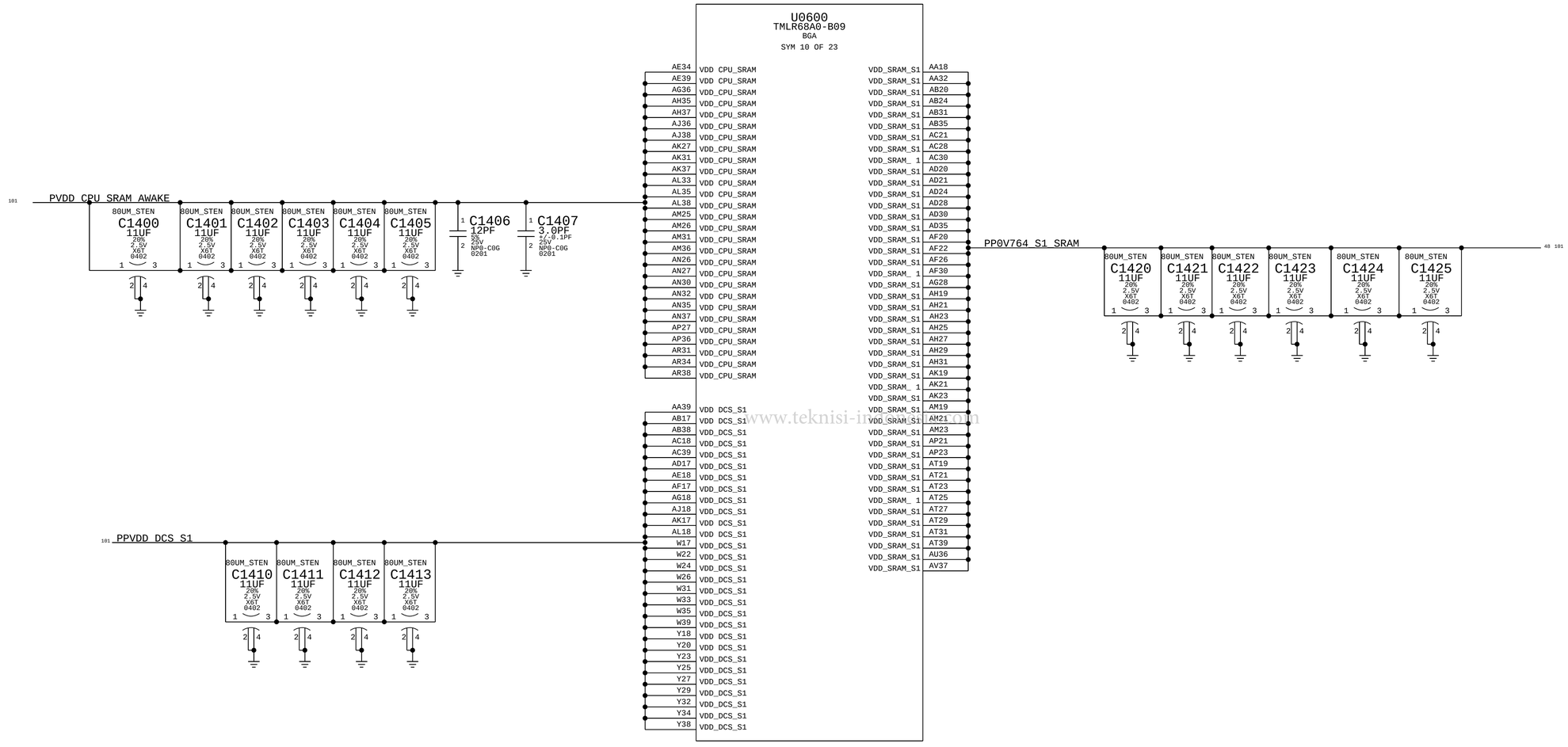
PAGE TITLE
SOC: POWER (SOC, CPU, GPU)

BOM_COST_GROUP=SOC

OK2INTEGRATE

SOC: POWER (SRAM, SOC)



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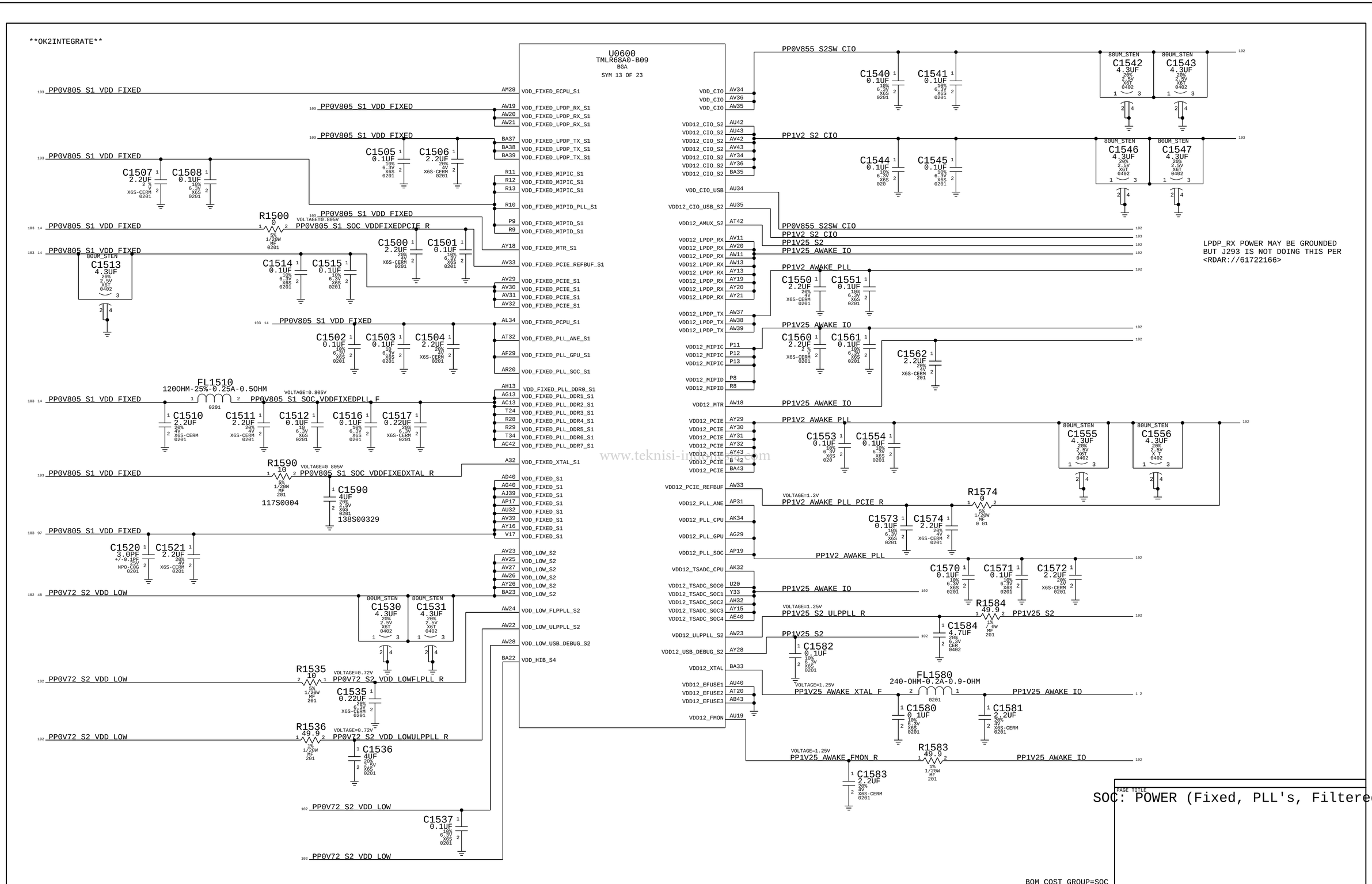
PAGE TITLE

SOC: POWER (SRAM)

BOM_COST_GROUP=SOC



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PAGE TITLE

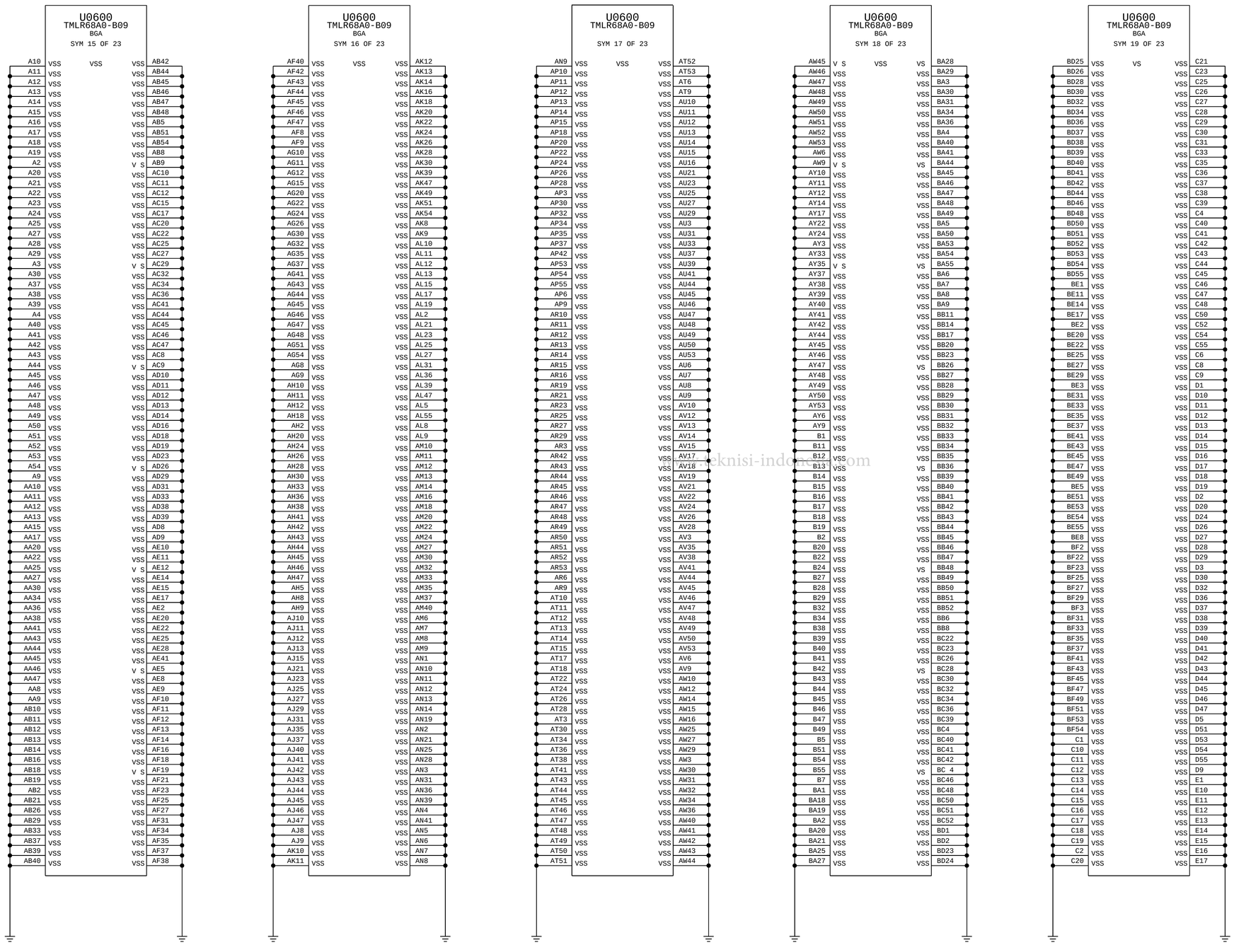
SOC: POWER (Fixed, PLL's, Filtered)

BOM_COST_GROUP=SOC

2 | 1

OK2INTEGRATE

SOC: GND (1)



teknisi-indonesia.com

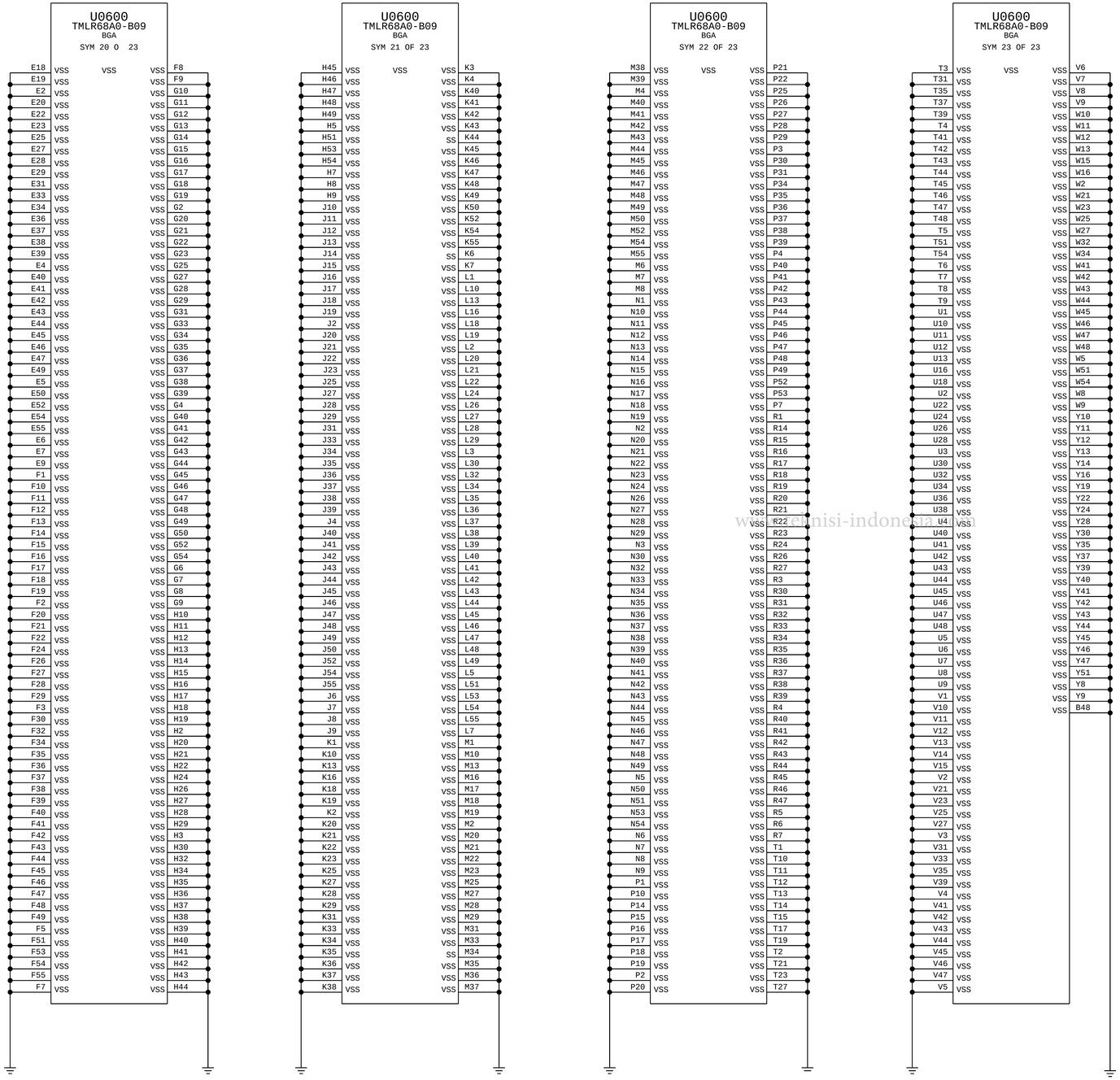
PAGE TITLE

SOC: GND

BOM_COST_GROUP=SOC

OK2INTEGRATE

SOC: GND (2)



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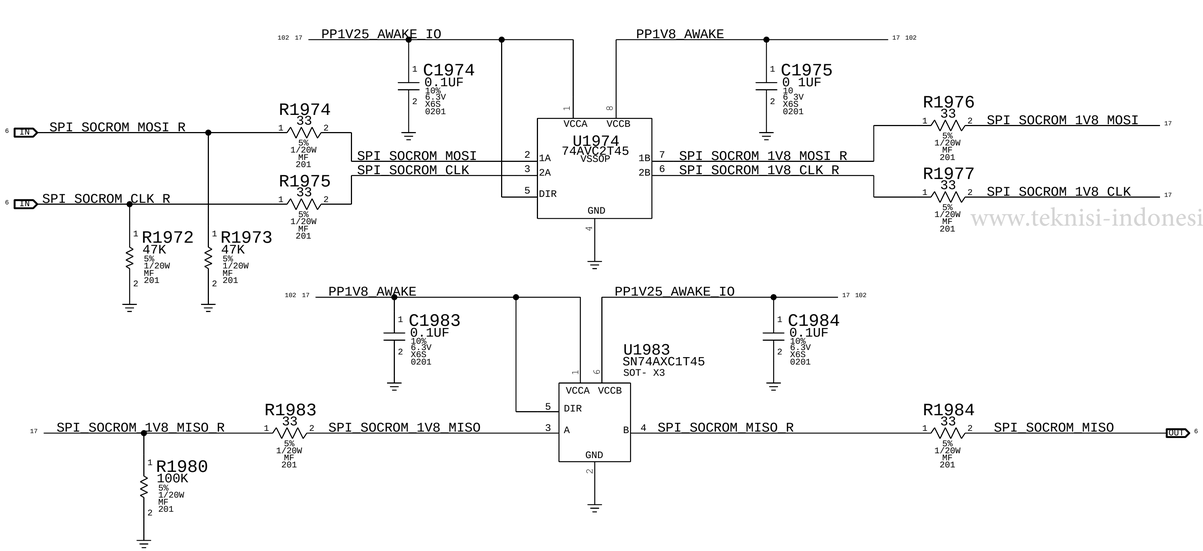
PAGE TITLE

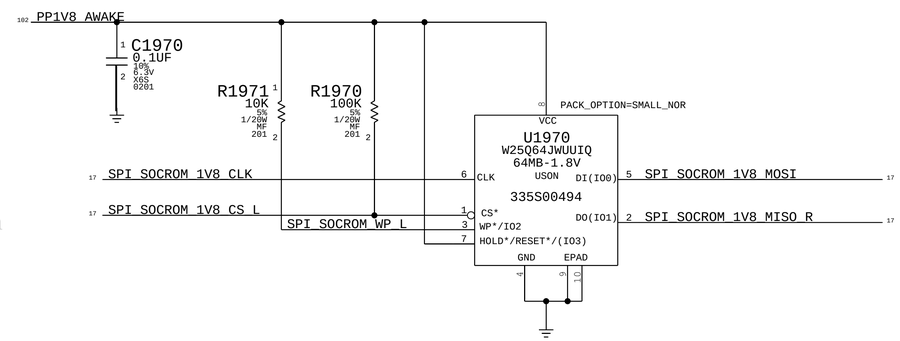
SOC: GND-2

BOM_COST_GROUP=SOC

OK2INTEGRATE

SPI NOR (1.8V 64 M-BIT)





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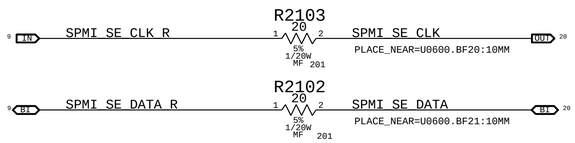
BOM_COST_GROUP=SOC

SYNC_MASTER=REF_SOC_H13G SYNC_DATE=01/27/2020

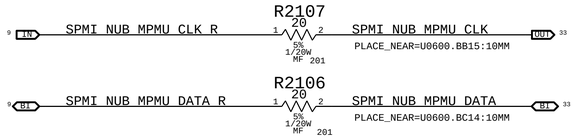
PAGE TITLE

SPI NOR

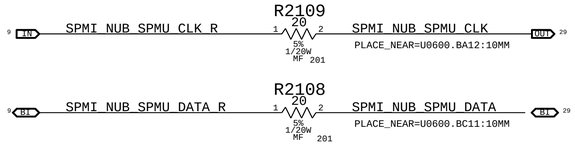
TGA SPMI SE SOURCE TERMINATIONS



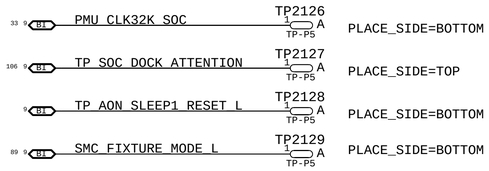
TGA SPMI MPMU SOURCE TERMINATIONS



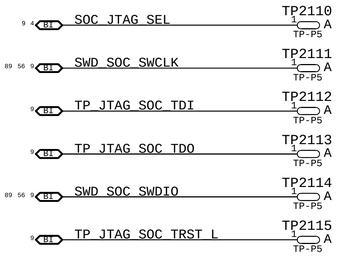
TGA SPMI SPMU SOURCE TERMINATIONS



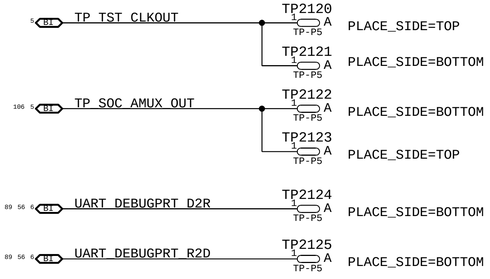
TGA MISC DEBUG TEST-POINTS



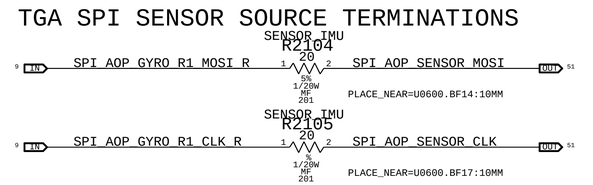
TGA JTAG TEST-POINTS



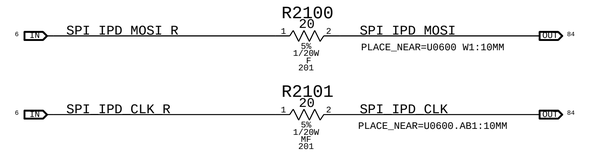
TGA DEBUG TEST-POINTS



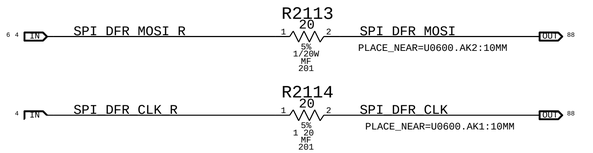
TGA SPI SENSOR SOURCE TERMINATIONS



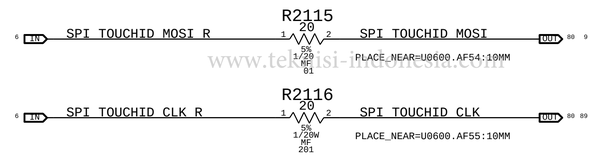
TGA SPI IPD SOURCE TERMINATIONS



TGA SPI DFR SOURCE TERMINATIONS



TGA SPI TOUCHID SOURCE TERMINATIONS



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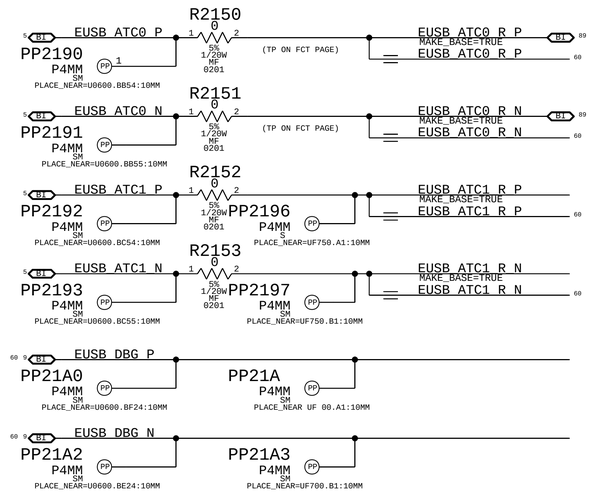
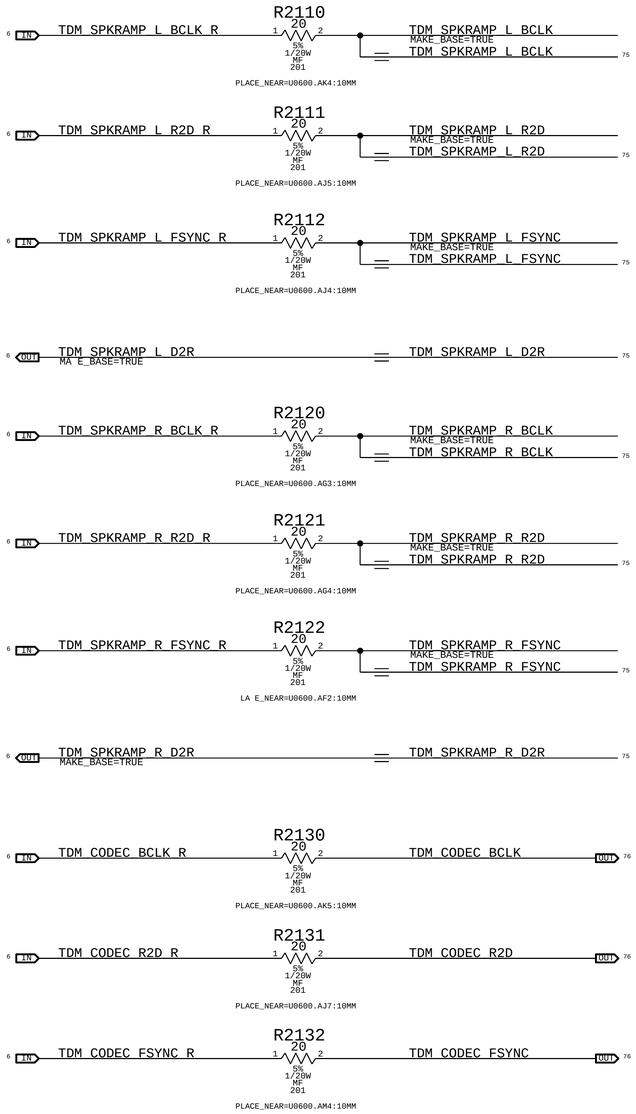
EUSB SERIES RESISTORS AND TEST POINTS



TGA 1V2 TDM SOURCE TERMINATIONS



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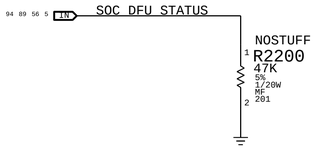
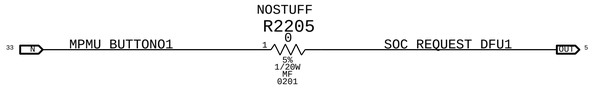
SYNC_MASTER=AITKEN_T668_MLB SYNC_DATE=09/18/2019

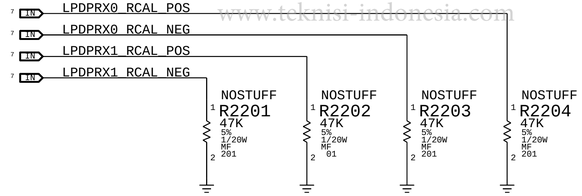
PAGE TITLE

PROJECT SUPPORT (1/2)





OPTION FOR SW TO READ POWER BUTTON, NOT USED



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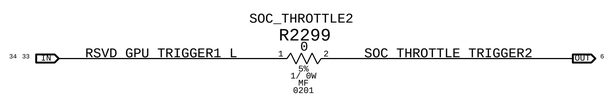


<RDAR://59954844>

SYNC_MASTER=AITKEN_T868_MLB SYNC_DATE=11/11/2019

PAGE TITLE

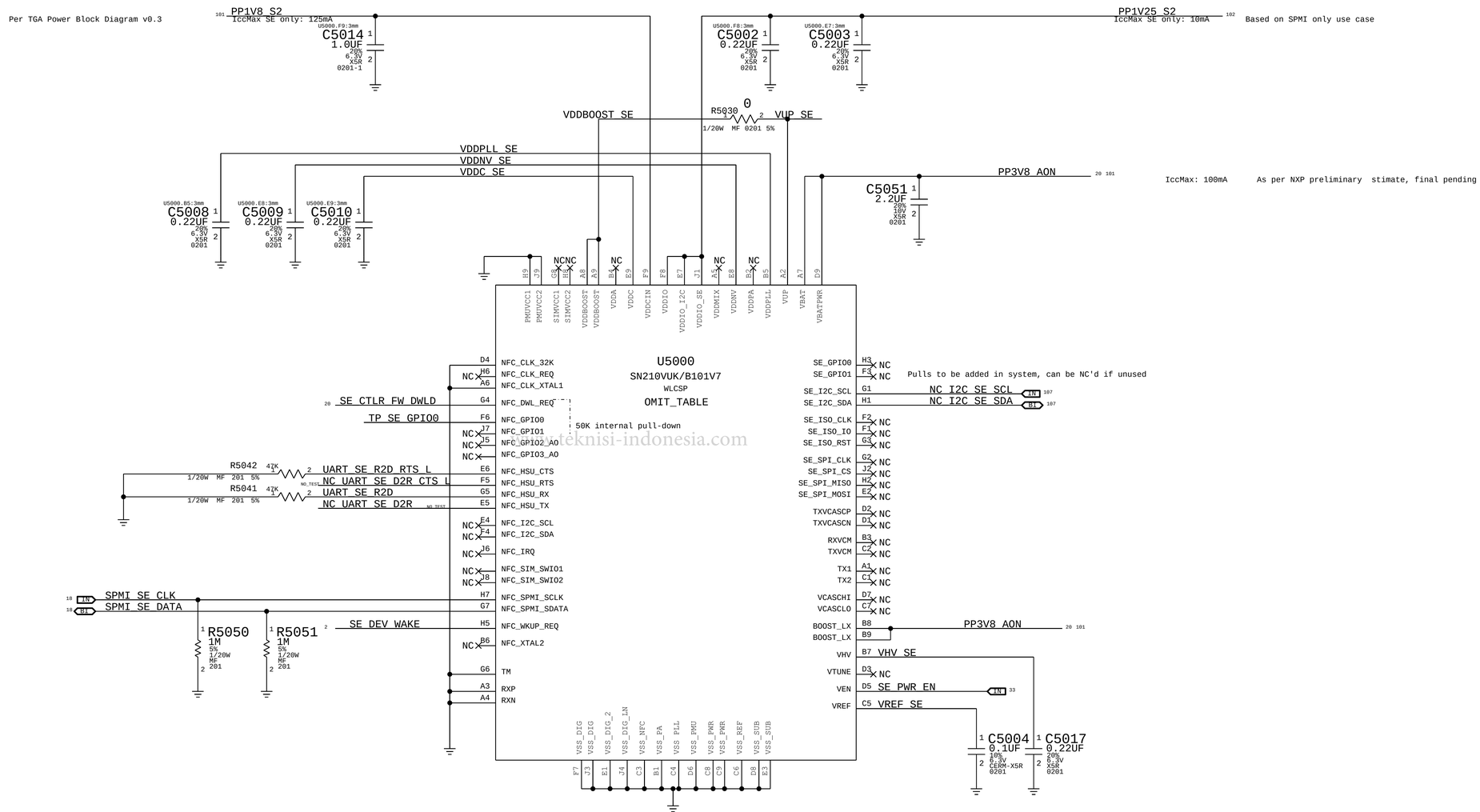
PROJECT SUPPORT (2/2)

BOM_COST_GROUP=SOC

Timing Requirements:
- VBAT supply ramp time: 20ms

Ceres - Secure Element

*** OK2INTEGRATE ***



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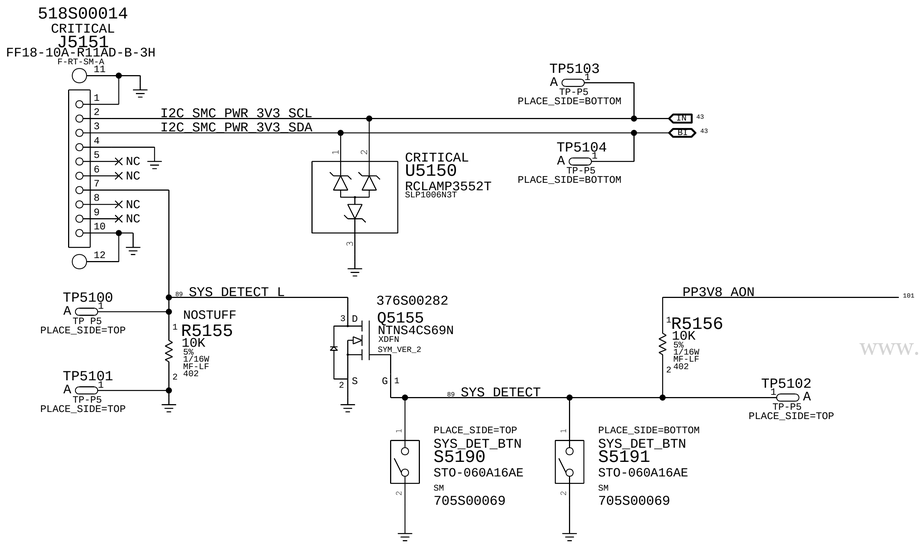
R5000 47K 5% 1/20W MF 201 — SE_CTLR_FW_DWLD
R5006 47K 5% 1/20W MF 201 — SE_DEV_WAKE

<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
<rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

BOM_COST_GROUP=SECURE ELEMENT

SYNC_MASTER=REF_SE_CERES SYNC_DATE=02/26/2020
PAGE TITLE
Secure Element

BATTERY (BMU) LOGIC CONNECTOR



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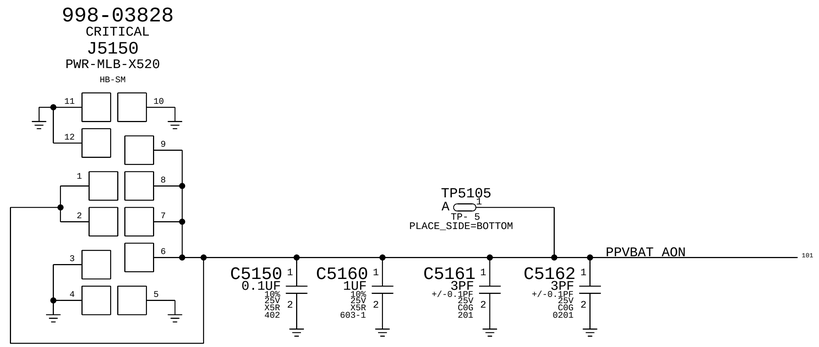
BATTERY (BMU) FLEX SOLDER PADS

BMU POWER FLEX IS SOLDERED TO MLB.



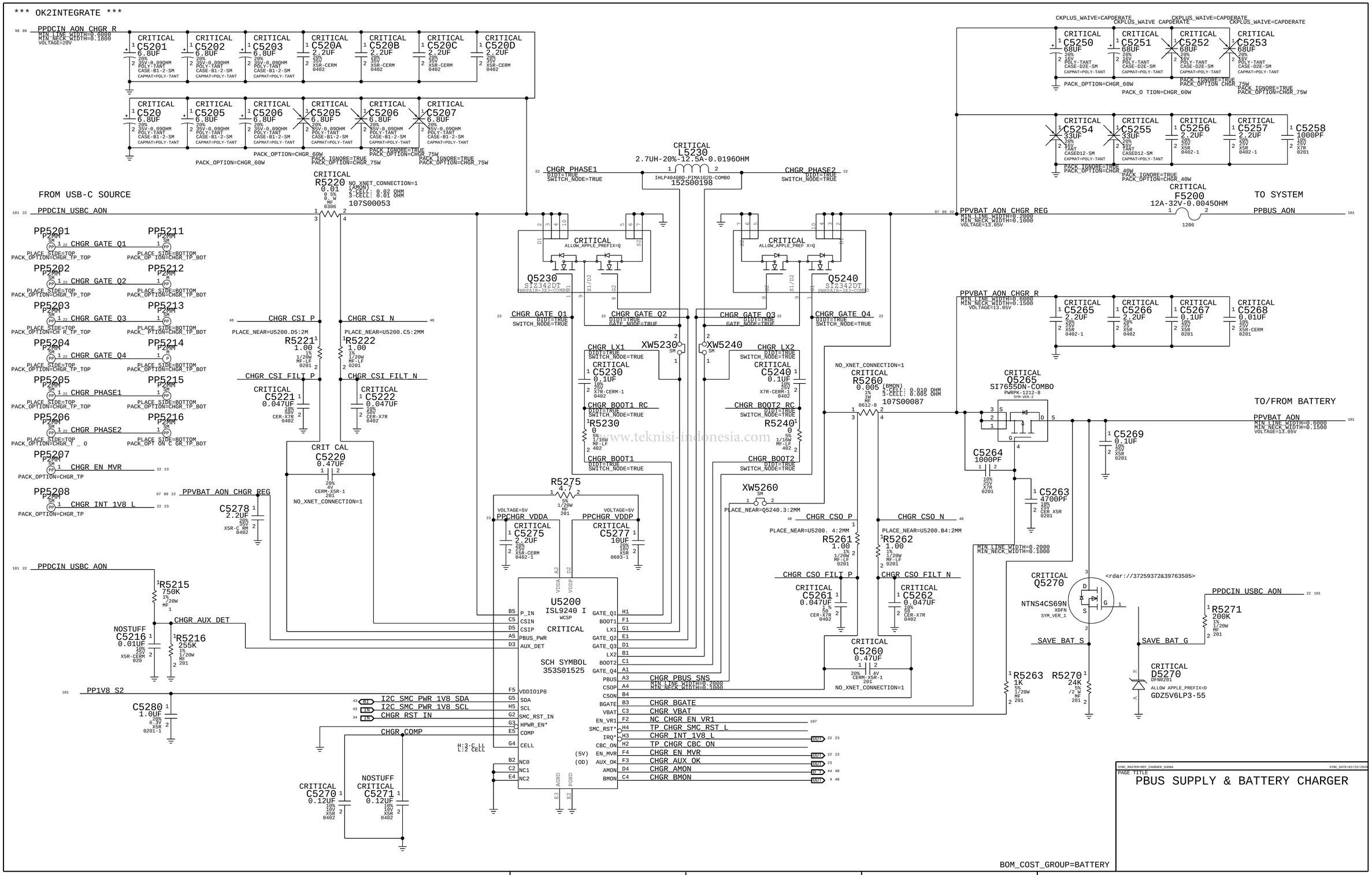
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA,FLEX,BMU PWR,X502	J5150	CRITICAL	

SYNC_MASTER=AITKEN_T668_MLB

PAGE TITLE

BATTERY CONNECTORS

BOM_COST_GROUP=BATTERY



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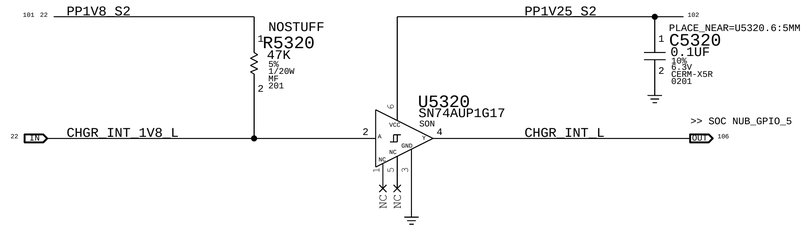
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

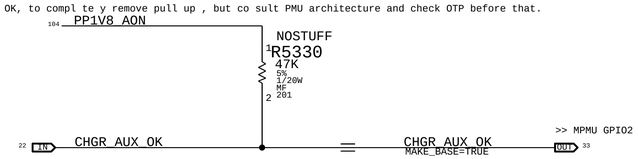
CHGR_INT_L Level Translation

Stuff R5320 in case, glitch during power sequencing is a concern.



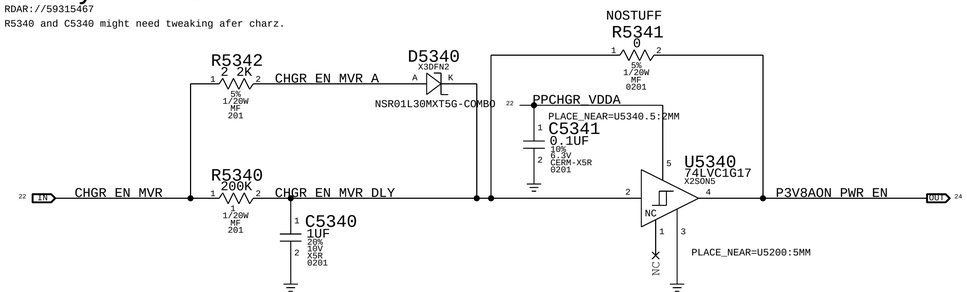
CHGR_AUX_OK Pull Up

Pull up to MPMU LDO9, or rely on MPMU internal pull up.
OK, to compl te y remove pull up , but co sult PMU architecture and check OTP before that.



Delay for 3.8V VR Enable

RDAR://59315467
R5340 and C5340 might need tweaking afer charz.



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SYNC_MASTER=REF_CHARGER_SUDNA SYNC_DATE=04/01/2020

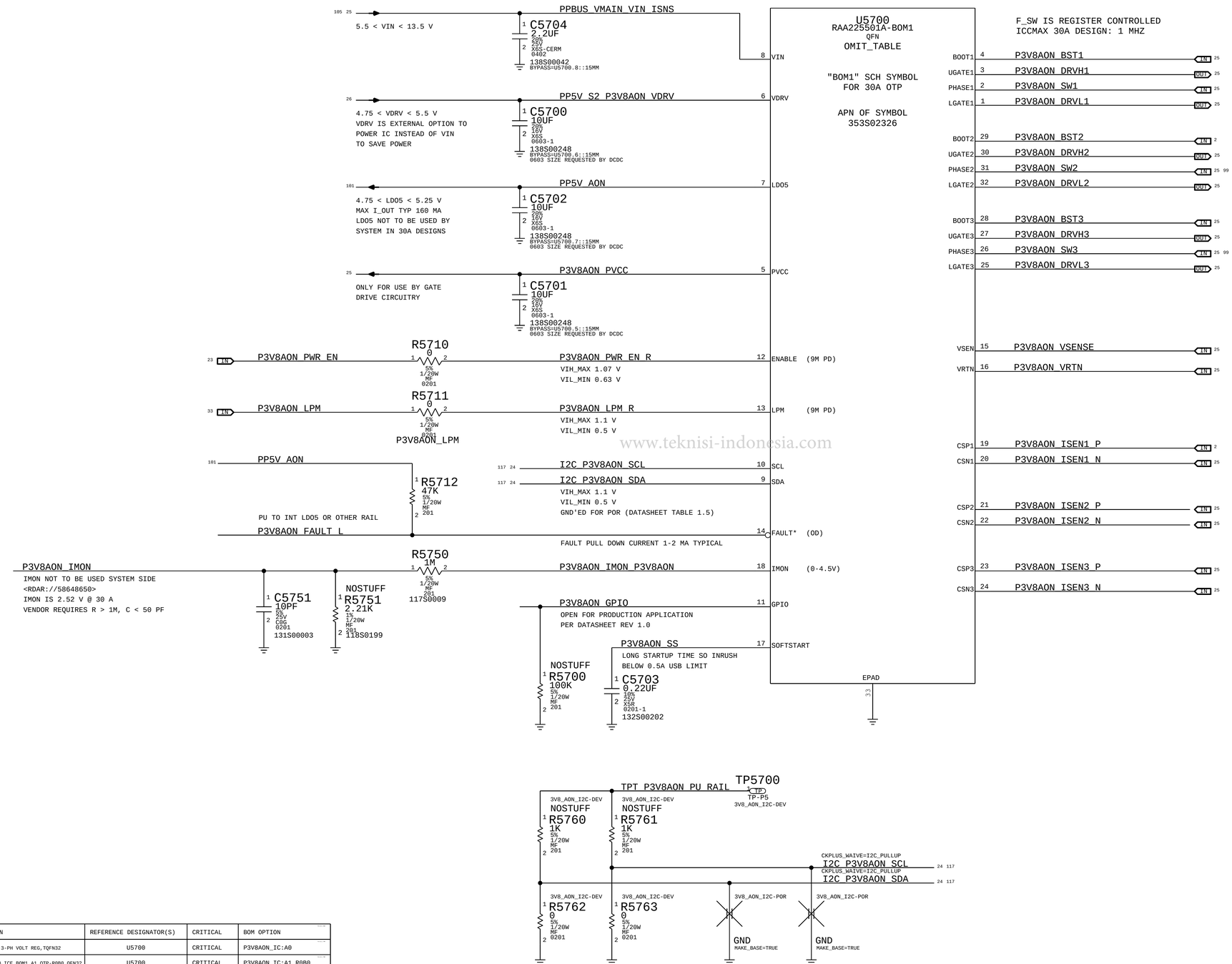
PAGE TITLE

BATTERY CHARGER SUPPORT

BOM_COST_GROUP=BATTERY

*** OK2RELEASE ***

3V8 AON CONTROLLER



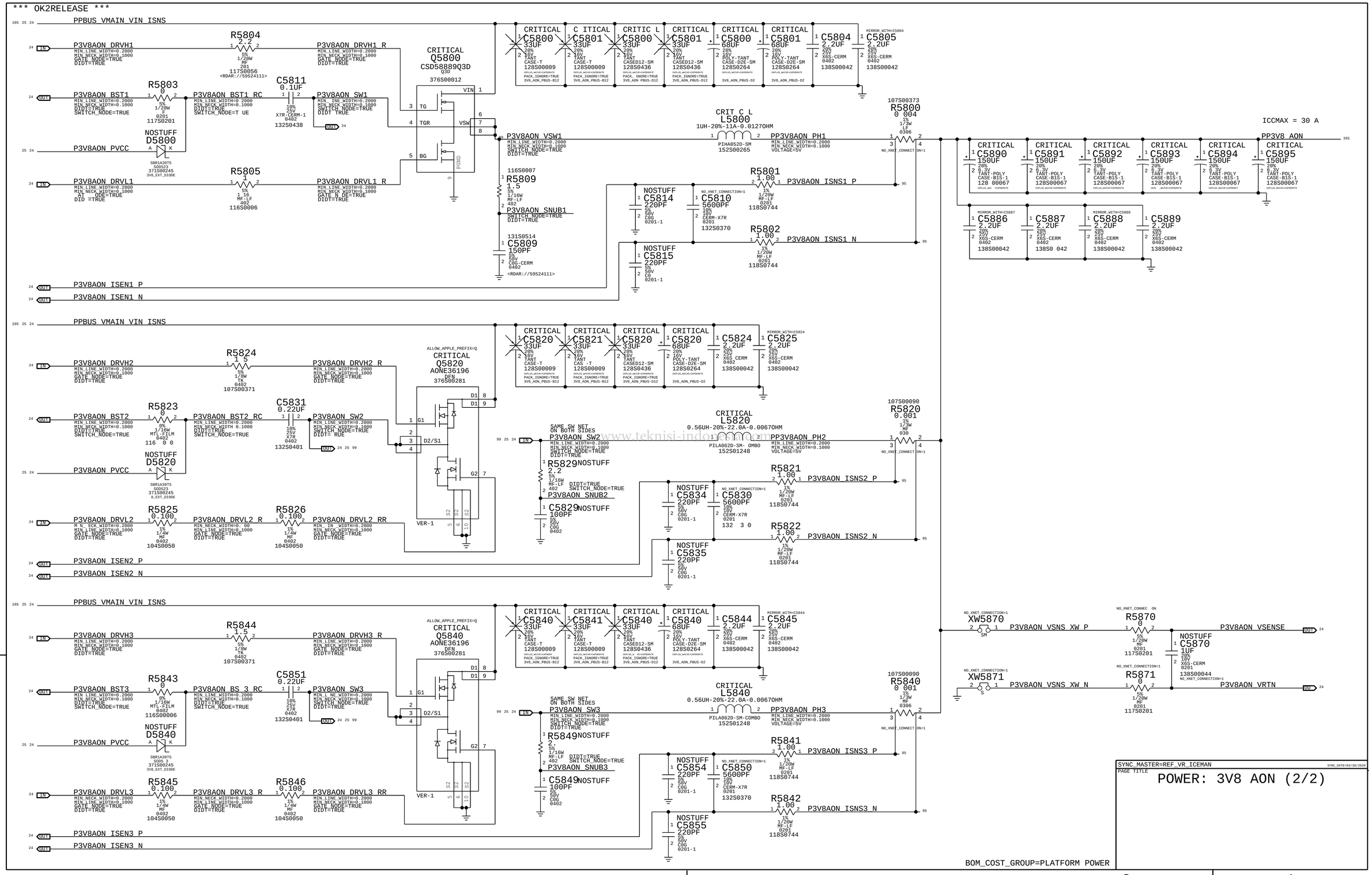
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02326	1	IC,RAA225501,3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8AON_IC:A0
353S02472	1	IC AA 5501B,ICE,BOM1,A1,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B0

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTE =REF_VR_ICEMAN SYNC_DATE=04/09/2020

PAGE TITLE

POWER: 3V8 AON (1/2)



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ZERO OHM RESISTOR TO ALLOW ACCESS TO VDRV

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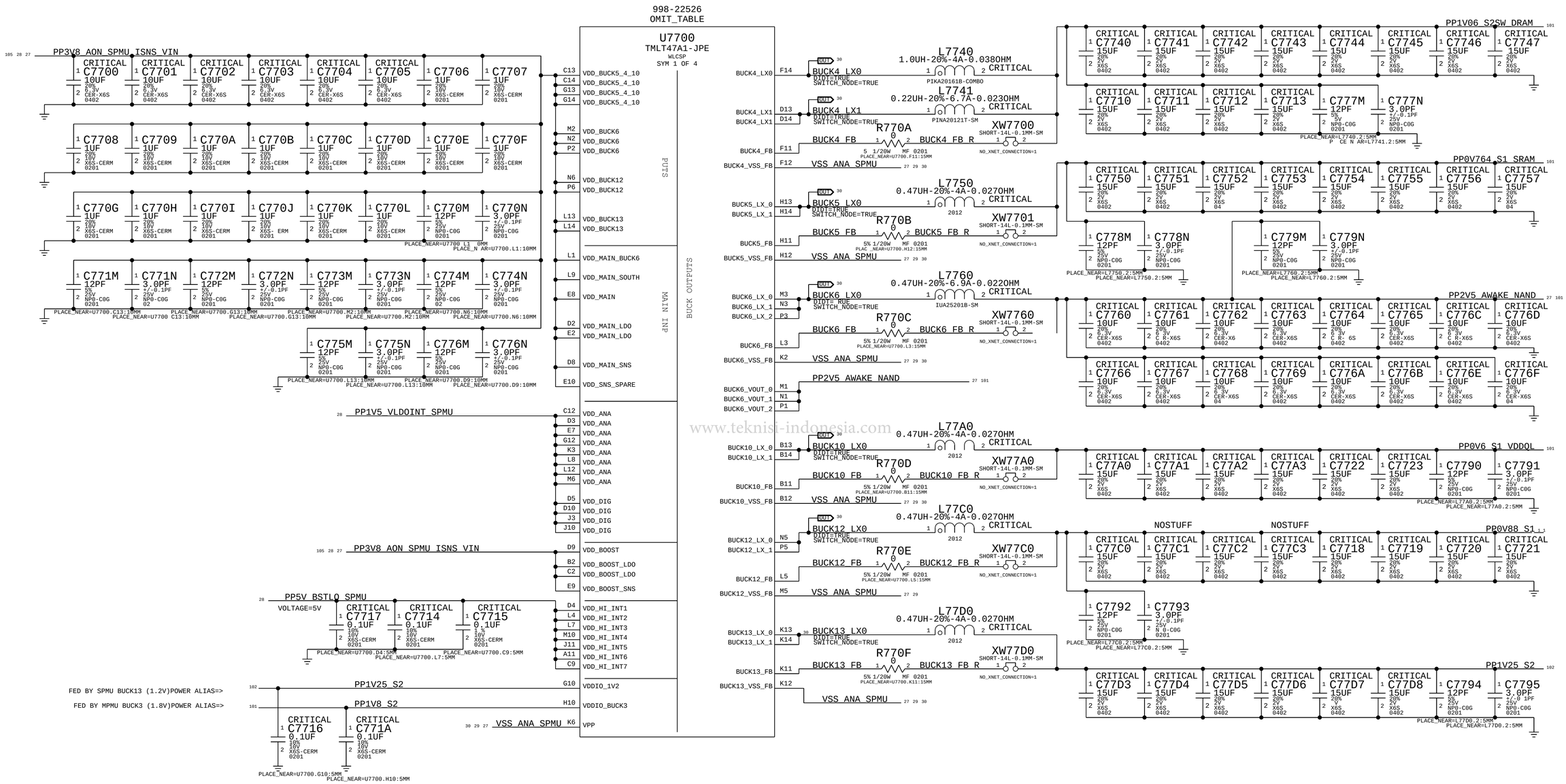
PAGE TITLE
POWER: 3V8 AON SUPPORT

BOM_COST_GROUP=PLATFORM POWER

SLAVE PMU INPUT POWER & BUCKS



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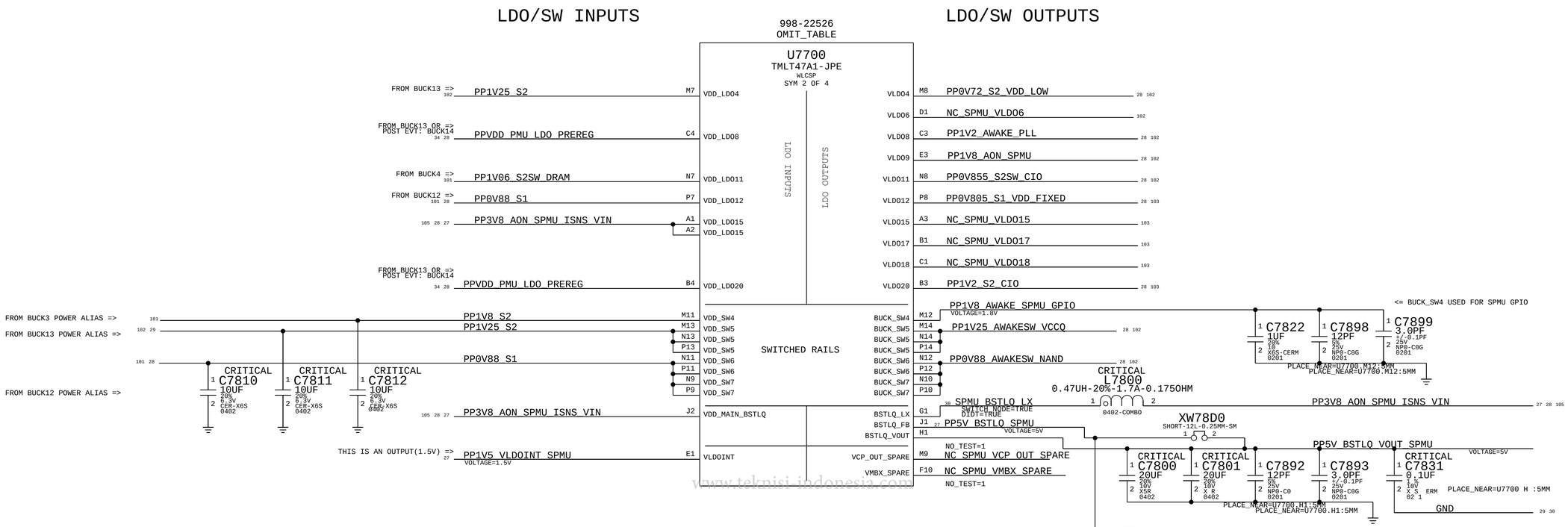
PAGE TITLE

PMU: SLAVE INPUT PWR & BUCKS

BOM COST GROUP=PLATFORM POWER

SLAVE PMU LDO, SWITCHES & BOOST



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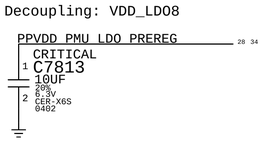
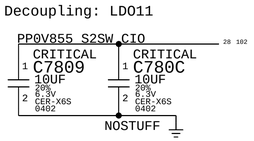
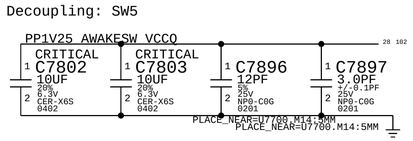
Decoupling: VDD_LDO8



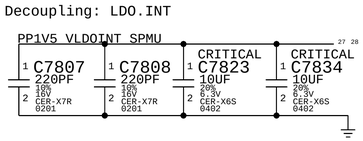
Decoupling: LDO11



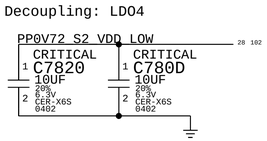
Decoupling: SW5



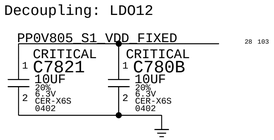
Decoupling: LDO.INT



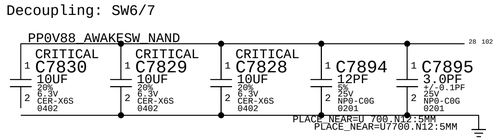
Decoupling: LDO4



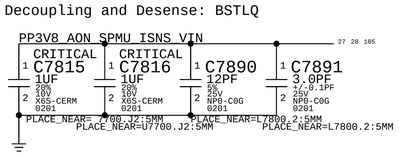
Decoupling: LDO12



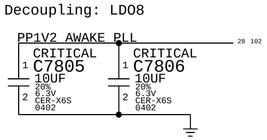
Decoupling: SW6/7



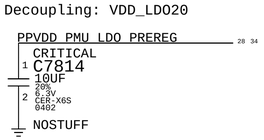
Decoupling and Desense: BSTLQ



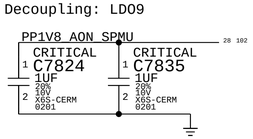
Decoupling: LDO8



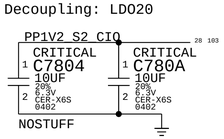
Decoupling: VDD_LDO20



Decoupling: LDO9



Decoupling: LDO20

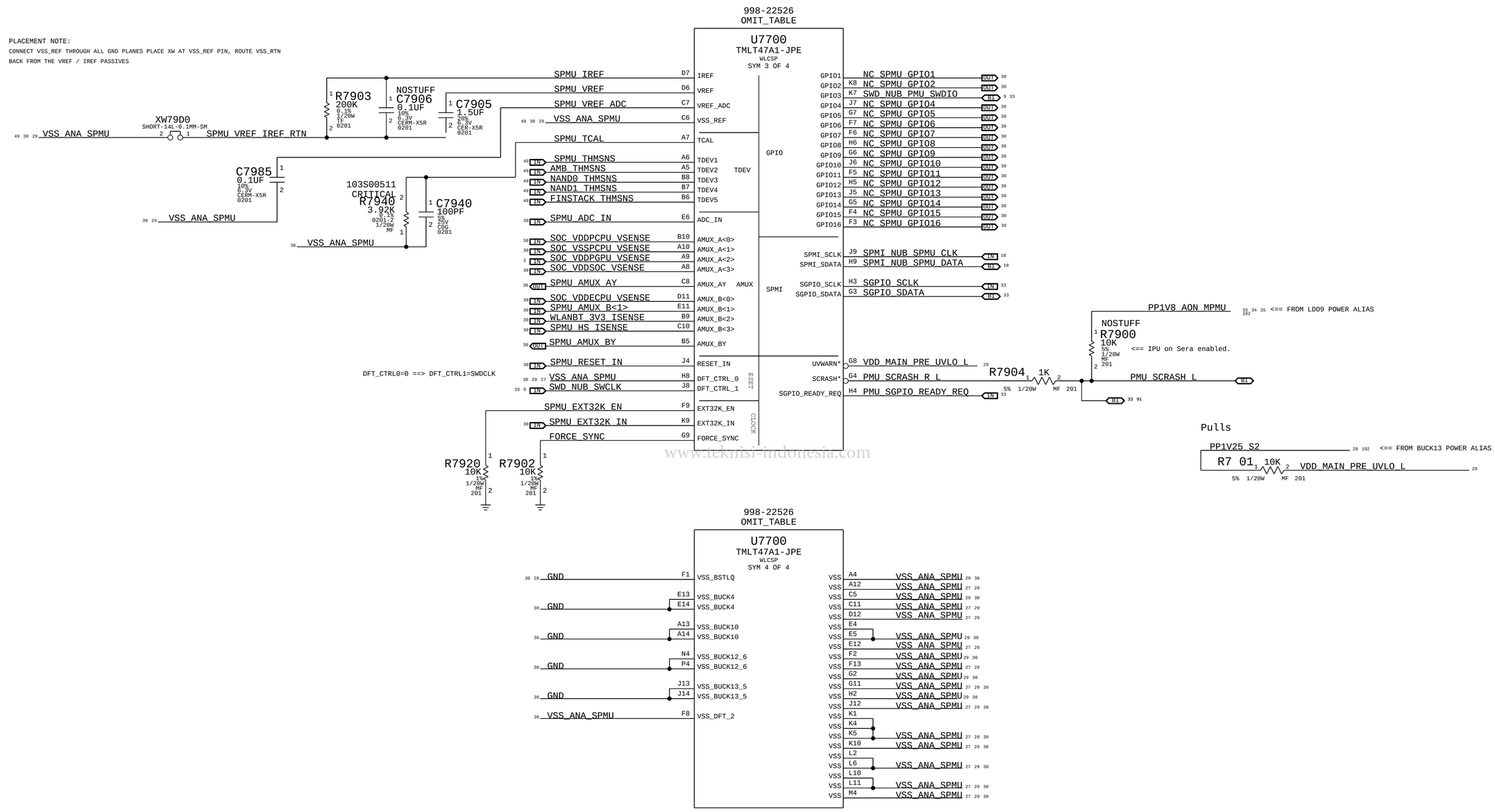


BOM COST GROUP=PLATFORM POWER

PAGE TITLE

PMU: SLAVE LDO

SLAVE PMU GND,ADC,& GPIO



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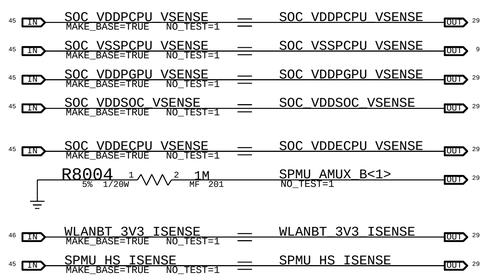
BOM COST GROUP=PLATFORM POWER

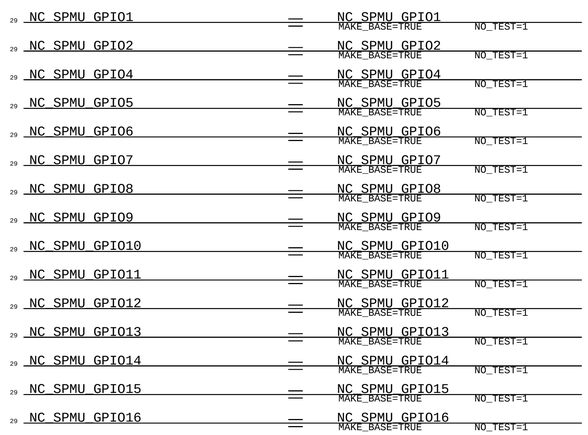
PAGE TITLE

PMU: SLAVE GPIO & GND

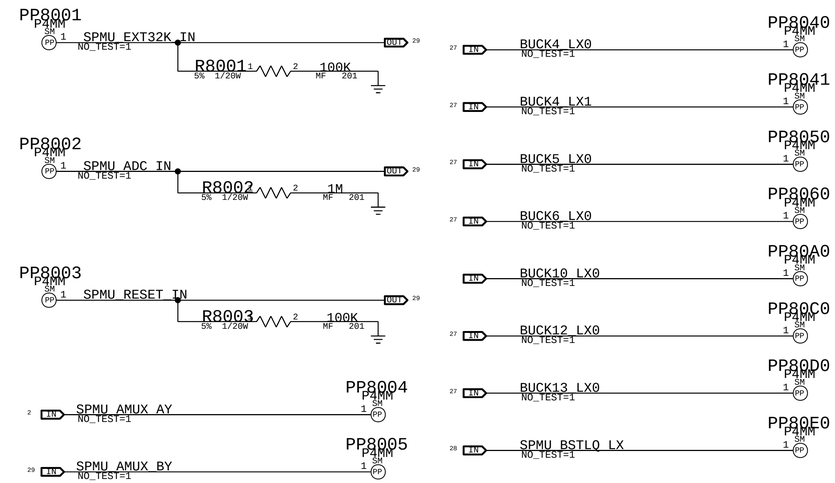
SLAVE PMU AMUX ALIAS



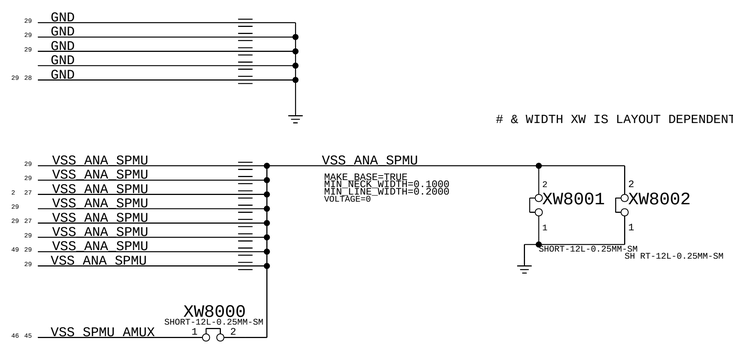
SLAVE PMU GPIOS



SLAVE PMU PROBE POINTS



VSS alias connection



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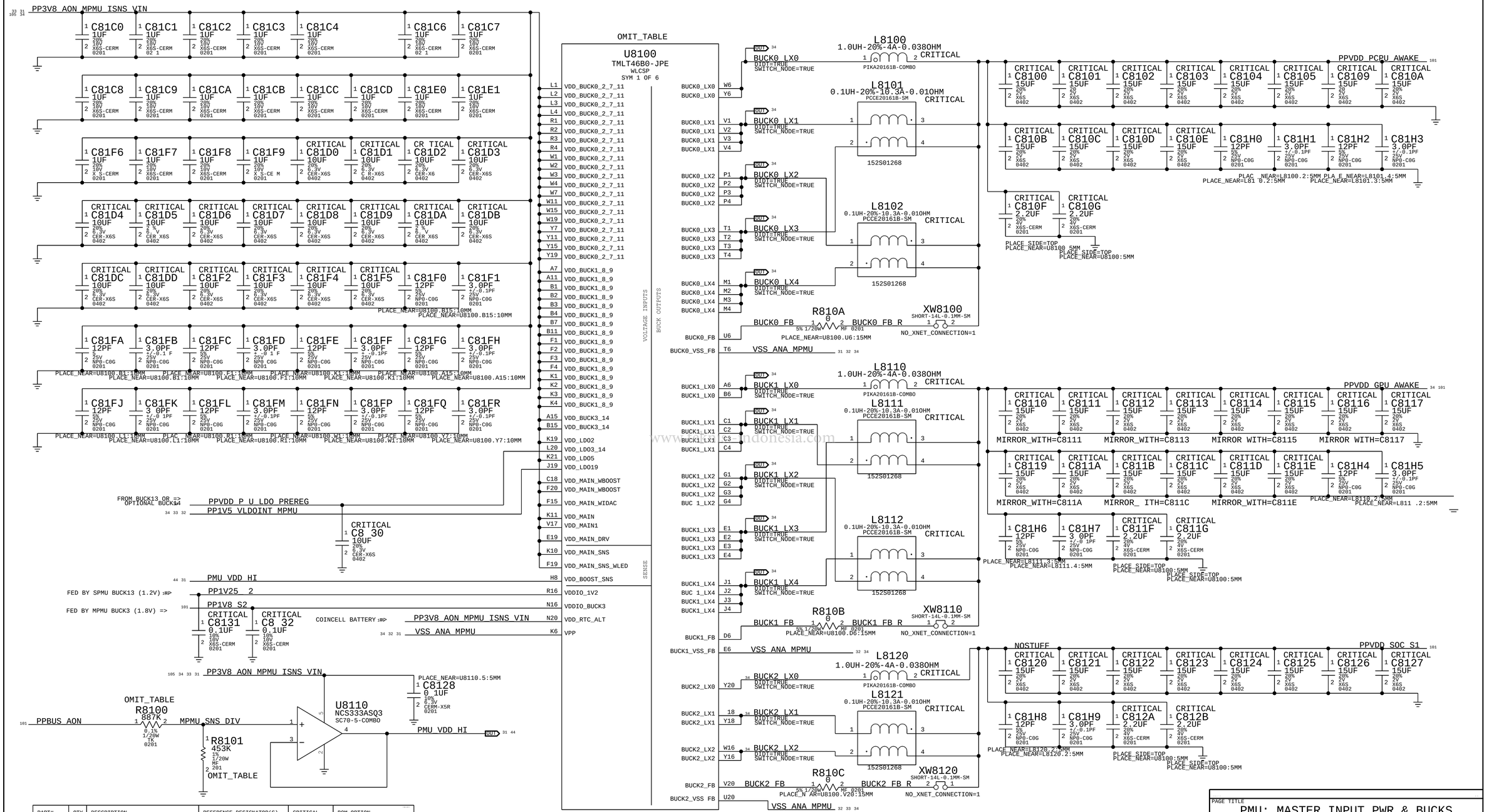
BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE

PMU: SLAVE SUPPORT

MASTER PMU BUCKS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
103S00385	1	RES,TK,887KOHM,0.1%,1/20W,0201	R8100	CRITICAL	PBUS_3S	<== FOR 3S BATTERY
103S00480	1	RES,MF,453KOHM,0.1%,1/20W,0201	R8101	CRITICAL	PBUS_3S	
103S00481	1	RES,MF,910KOHM,0.1% 1/20W,0201	R8100	CRITICAL	PBUS_12VDCIN	<== FOR 12V DCIN
103S00482	1	RES,MF,348KOHM,0.1%,1/ 0W,0201	R8101	CRITICAL	PBUS_12VDCIN	
103S00385	1	RES,TK,887KOHM,0.1%,1/20W,0201	R8100	CRITICAL	PBUS_15P8VDCIN	<== FOR 15.8V DCIN
103S0413	1	RES,MF,180KOHM,0.1%,1/20 0 1	R8101	CRITICAL	PBUS_ 5 8VDCIN	

PAGE TITLE

PMU: MASTER INPUT PWR & BUCKS

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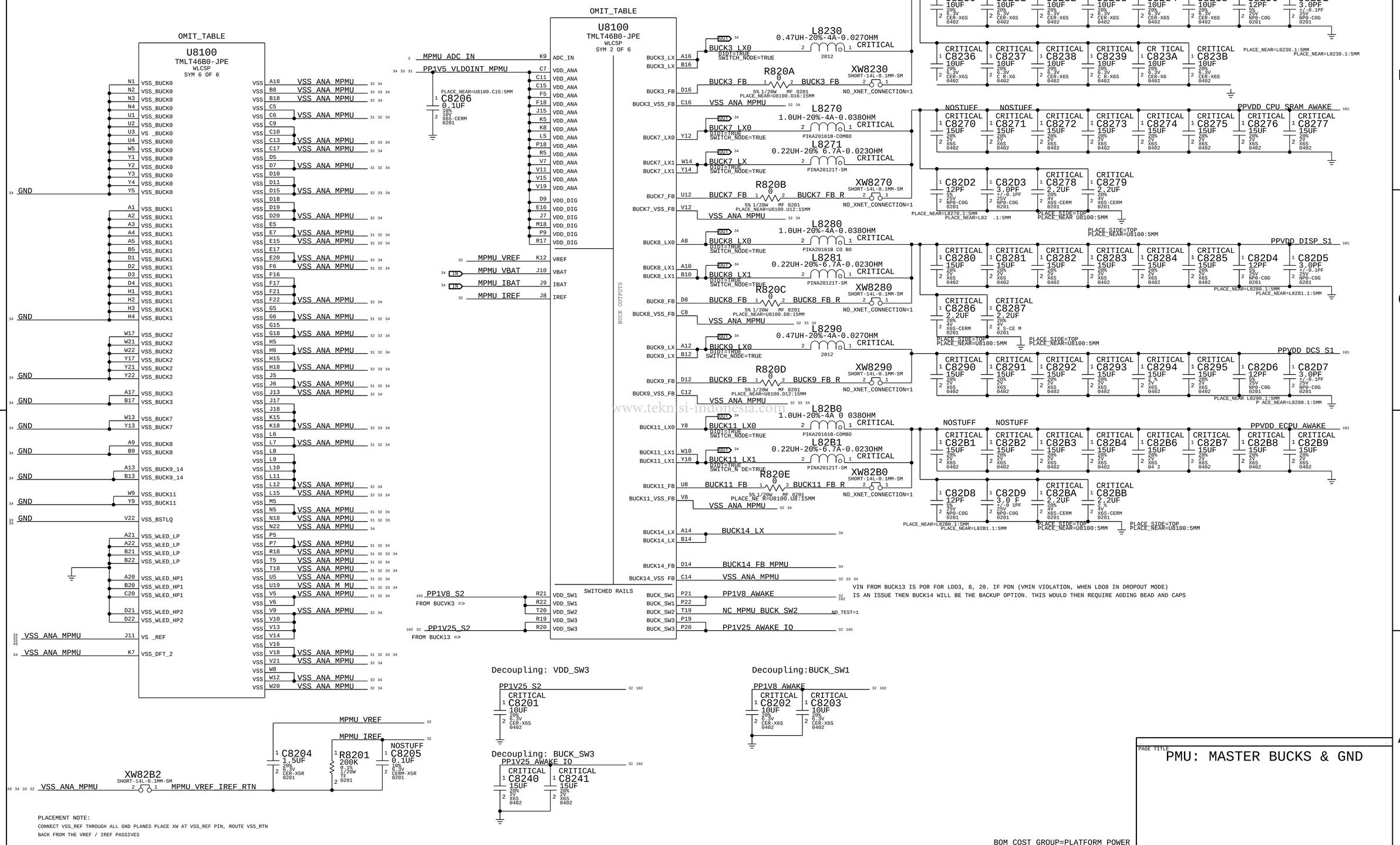
MASTER PMU BUCKS & GND



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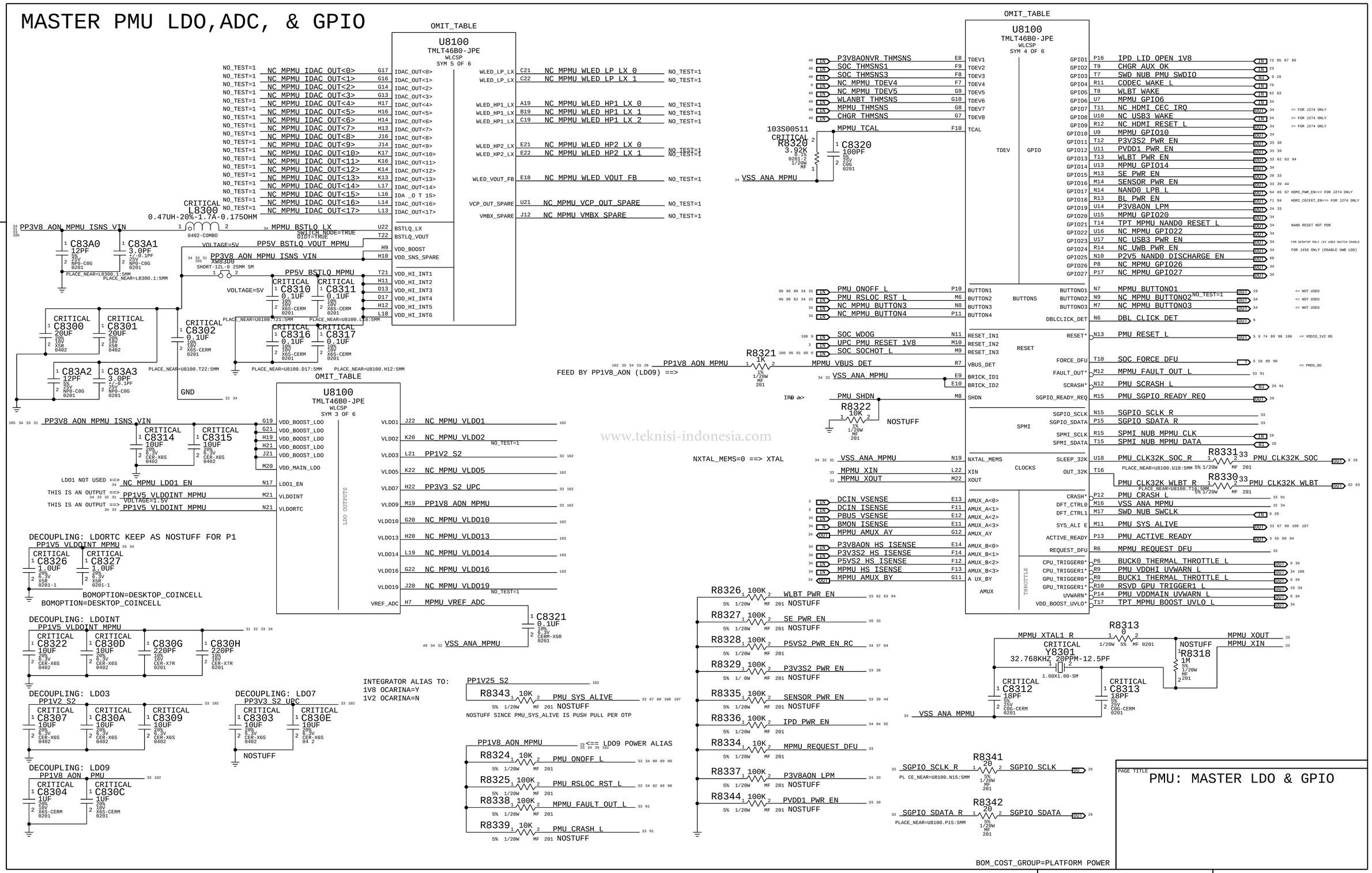
MASTER PMU LDO,ADC, & GPIO



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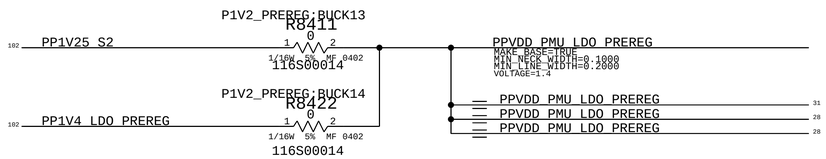
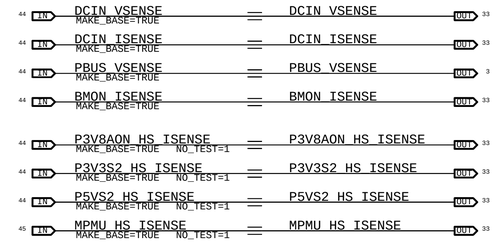
PP1V2 LDO VDD IN option (LDO3, 8, 20)

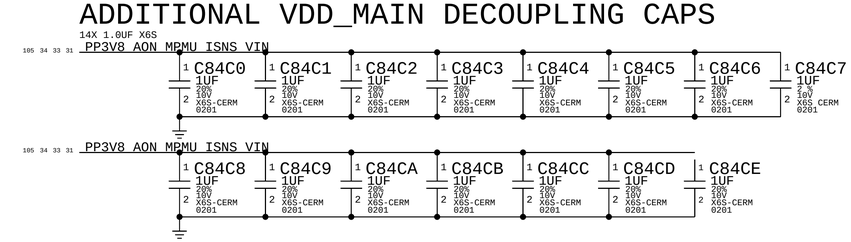
Stuff R8422 for BUCK14 pre-regulator (Proto2 and later)



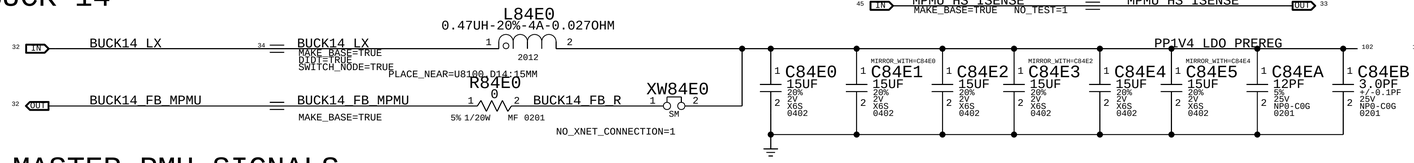
MASTER PMU AMUX ALIAS



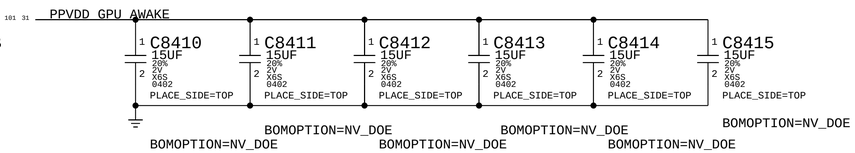
ADDITIONAL VDD_MAIN DECOUPLING CAPS



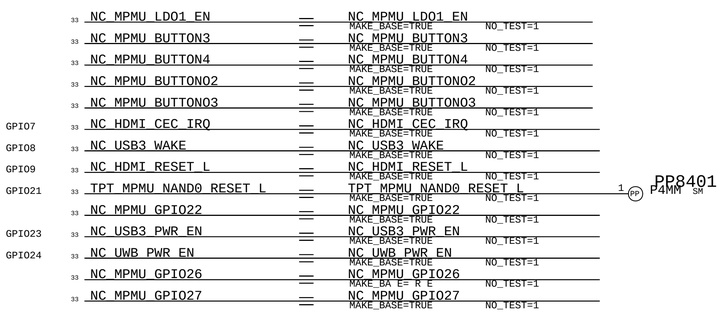
BUCK 14



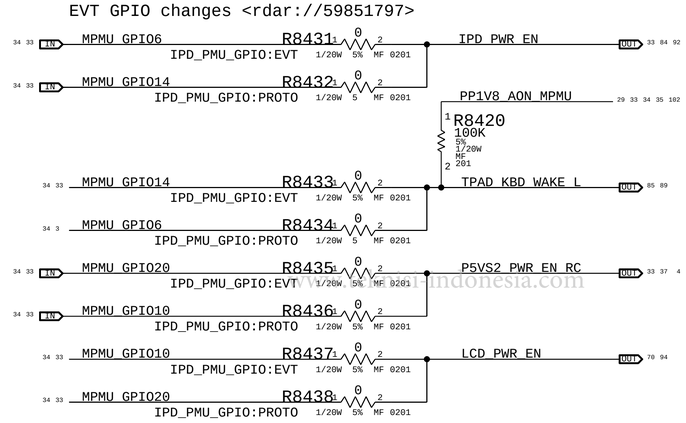
GPU RAIL N&V DOE CAPS



MASTER PMU SIGNALS



EVT GPIO changes <rdar://59851797>



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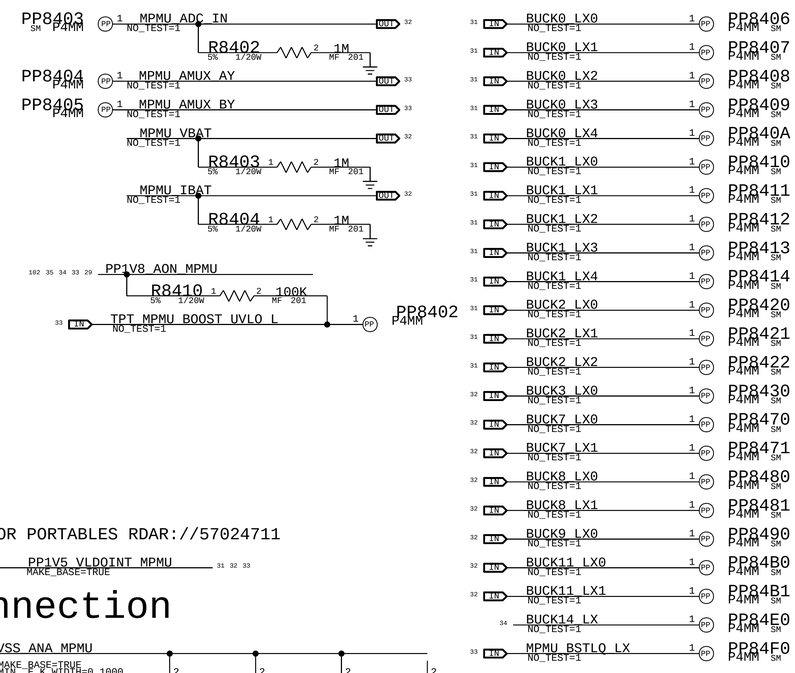
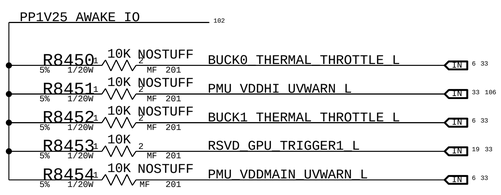
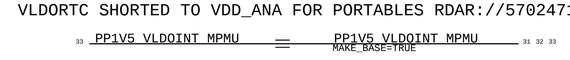
MASTER PMU PROBE POINTS



EXTERNAL PULL UPS FOR THROTTLE SIGNALS: SOC HAS IPU



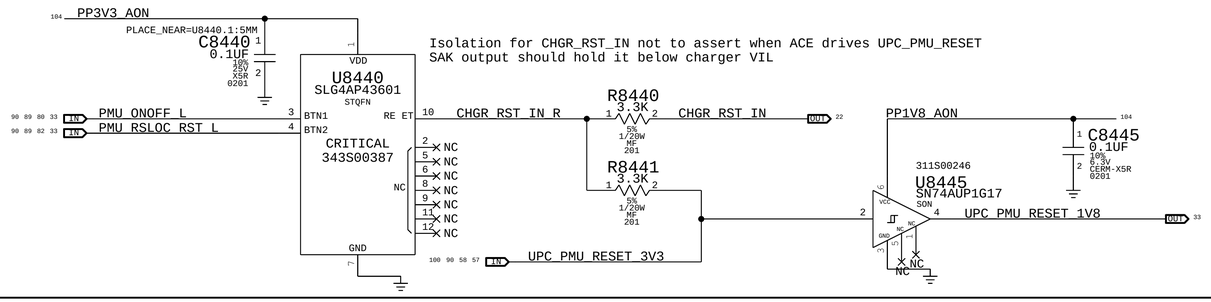
VLDORTC SHORTED TO VDD_ANA FOR PORTABLES RDAR://57024711



CHARGER RESET CIRCUIT

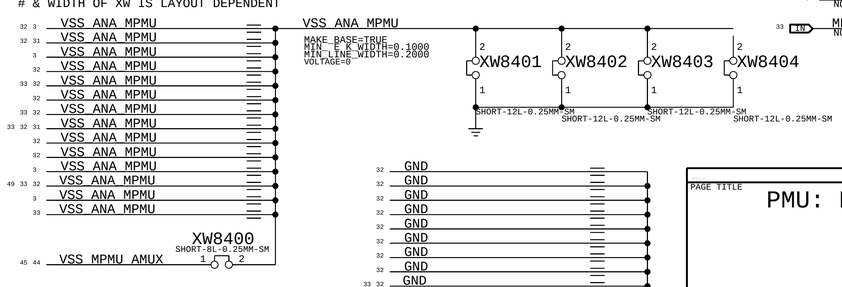
RIGHT SHIFT & LEFT OPTION CONTROL (RSLOC)
FOLLOWED BY ON-OFF BUTTON PRESS.
NEW APN 343S00387 can take 1.8V as BTN1/2 inputs.

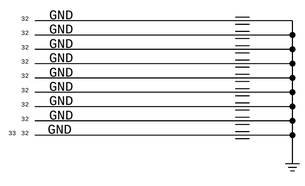
Isolation for CHGR_RST_IN not to assert when ACE drives UPC_PMU_RESET
SAK output should hold it below charger VIL



VSS alias connection

& WIDTH OF XW IS LAYOUT DEPENDENT



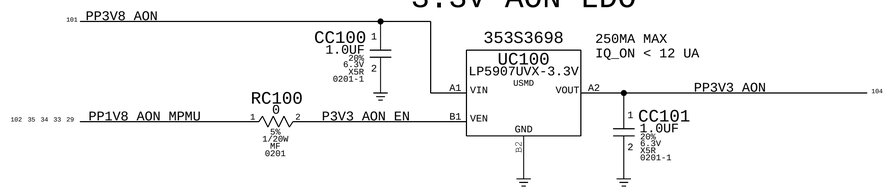


BOM_COST_GROUP=PLATFORM POWER

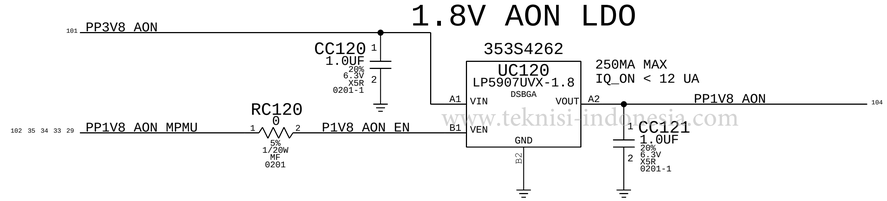
PAGE TITLE

PMU: MASTER SUPPORT

3.3V AON LDO



1.8V AON LDO



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BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=KEI_T668_MLB SYNC_DATE=09/23/2019

PAGE TITLE

POWER: EXTERNAL LDO

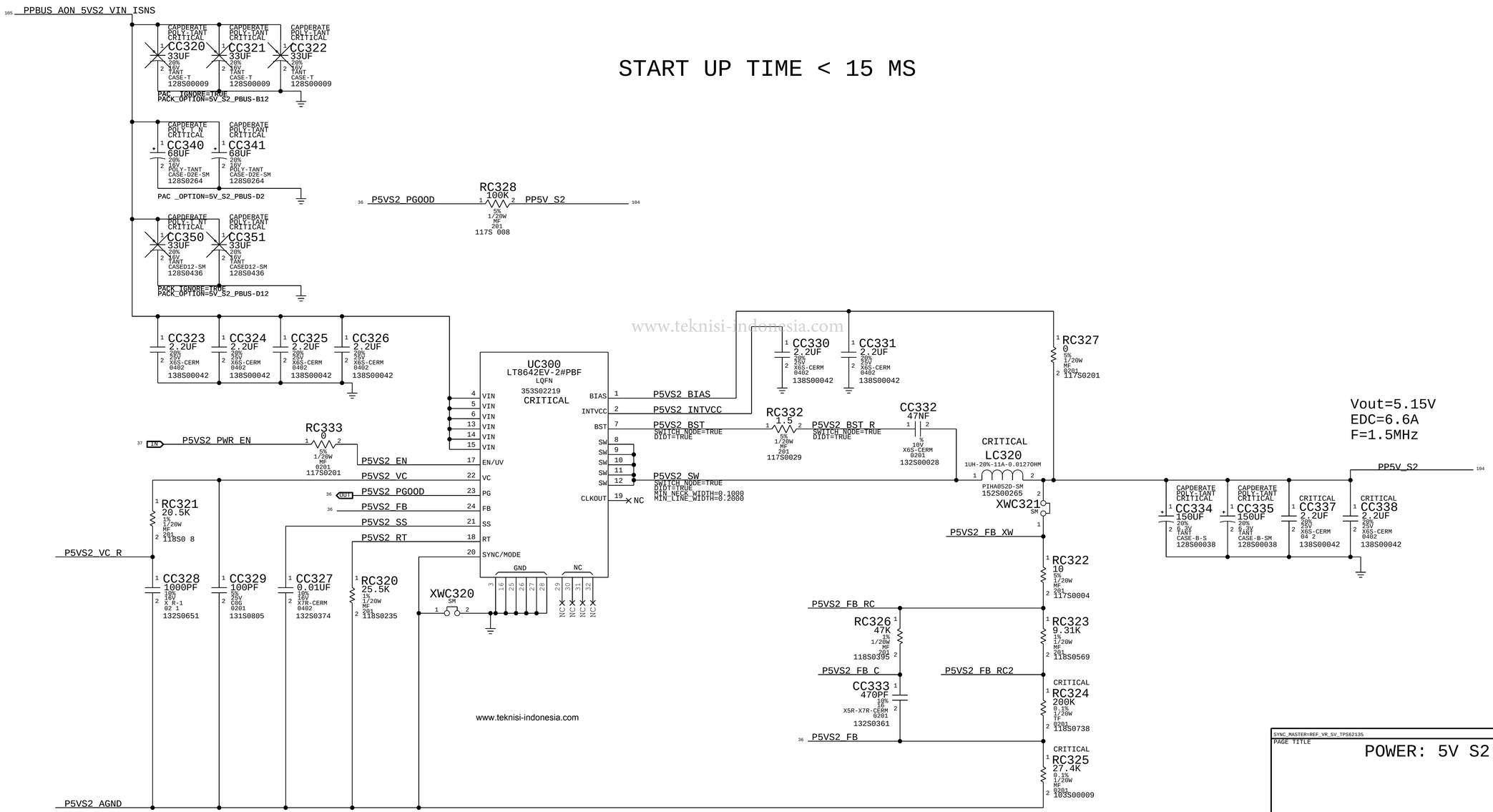
* OK2INTEGRATE *

5V_S2 Voltage Regulator

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=5V_S2_PBUS-B12
PACK_OPTION=5V_S2_PBUS-D2
PACK_OPTION=5V_S2_PBUS-D12

START UP TIME < 15 MS



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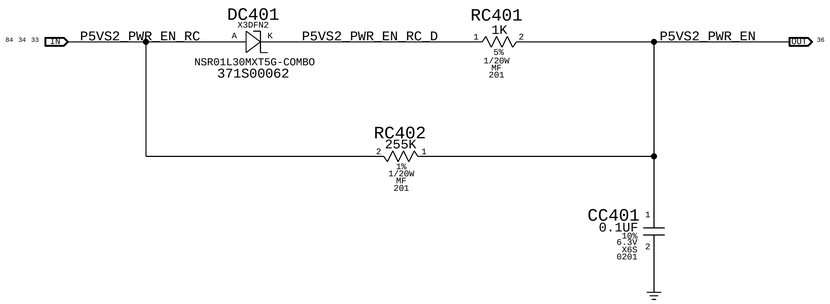
5VS2_EN TURN OFF DELAY 13-16MS



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SYNC_MASTER=T660_MLB SYNC_DATE=03/26/2020

PAGE TITLE

POWER: 5V S2 SUPPORT

A

BOM_COST_GROUP=PLATFORM POWER

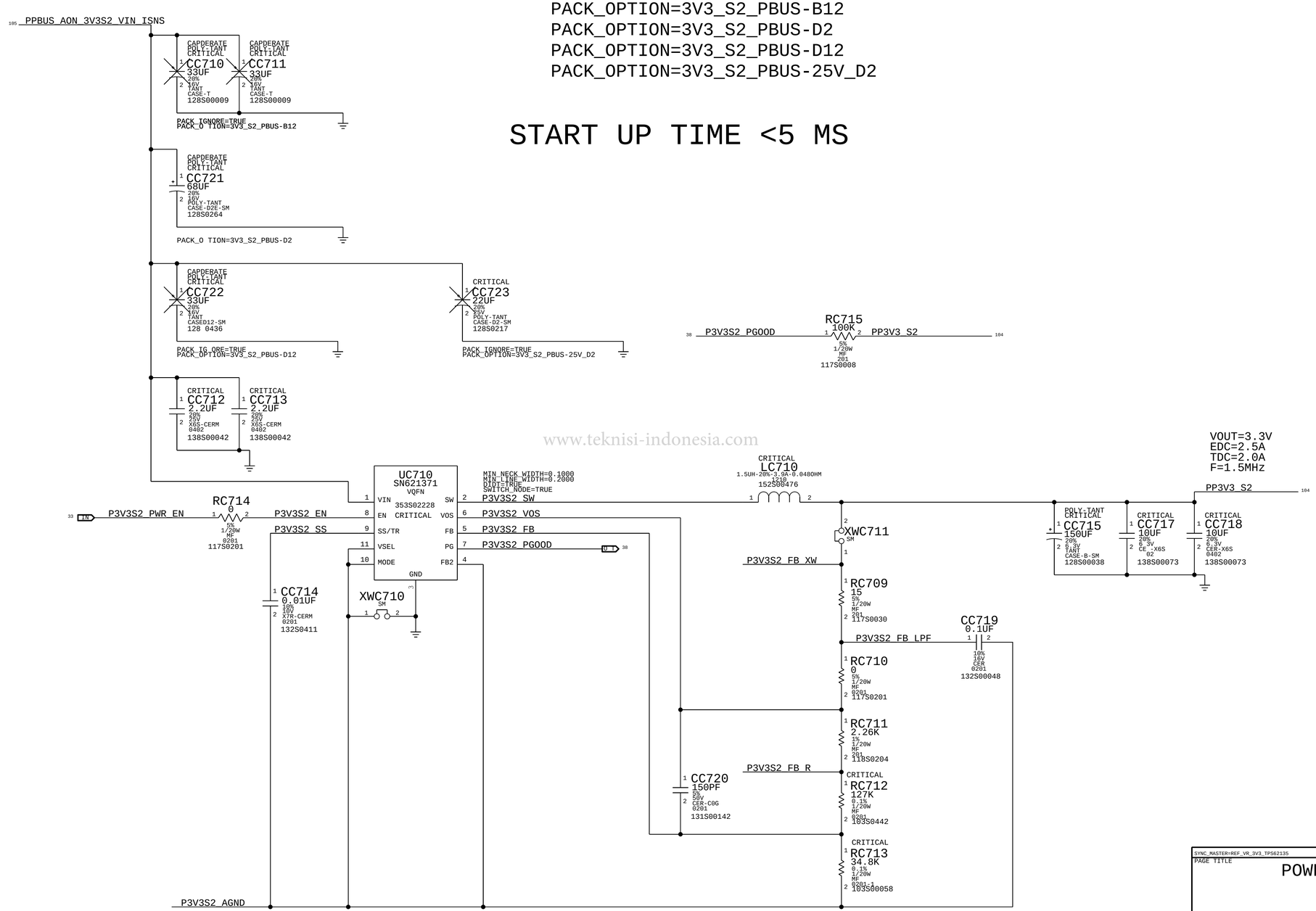
* OK2INTEGRATE *

3V3_S2 VR

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=3V3_S2_PBUS-B12
PACK_OPTION=3V3_S2_PBUS-D2
PACK_OPTION=3V3_S2_PBUS-D12
PACK_OPTION=3V3_S2_PBUS-25V_D2

START UP TIME <5 MS



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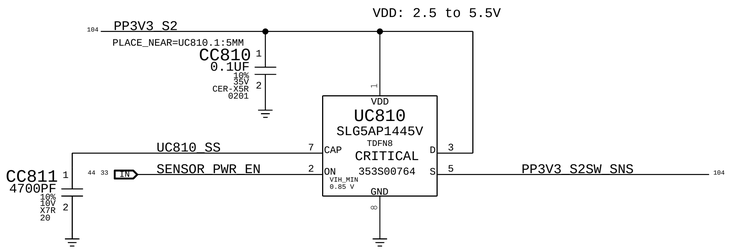
SYNC_MASTER=REF_VR_3V3_TPS62135 SYNC_DATE=01/09/2020

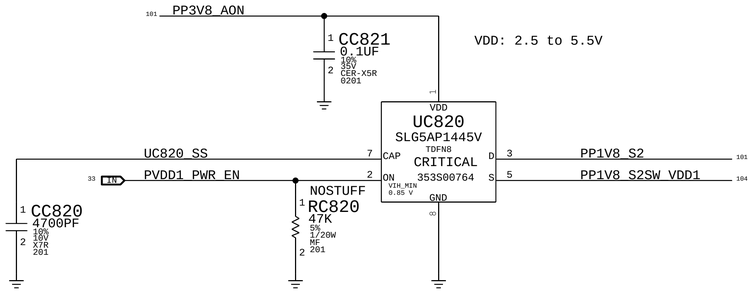
PAGE TITLE

POWER: 3V3 S2

3.3V SENSOR SWITCH (WIP)



1V8_S2 SWITCH (FROM J213 1V8 G3S)



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SYNC_MASTER=WEI_T668_MLB SYNC_DATE=09/10/2019

PAGE TITLE

POWER: FETS

BOM_COST_GROUP=PLATFORM POWER

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SYNC_MASTER=WEI_T668_MLB SYNC_DATE=09/10/2019

PAGE TITLE

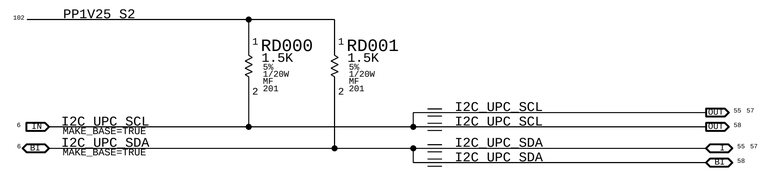
POWER: SUPPORT

BOM_COST_GROUP=PLATFORM POWER

SIO I2C0

DIAGS BUS: 0

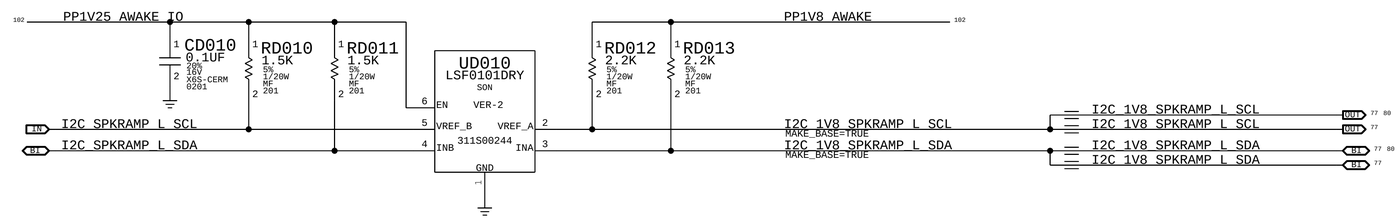
DEVICE	7-BIT
ACE 0	0X38
ACE 1	0X3F



SIO I2C1

DIAGS BUS: 1

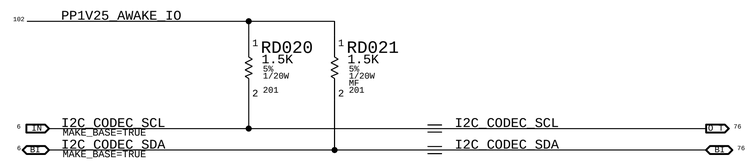
DEVICE	7-BIT
SPKRAMP L (A)	0X31
SPKRAMP L (B)	0X32



SIO I2C2

DIAGS BUS: 2

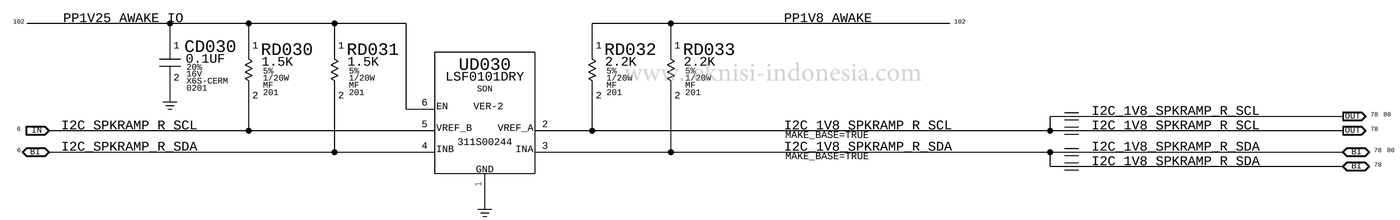
DEVICE	7-BIT
CS42L83A	0X48



SIO I2C3

DIAGS BUS: 3

DEVICE	7-BIT
SPKRAMP R (D)	0X34
SPKRAMP R (E)	0X35



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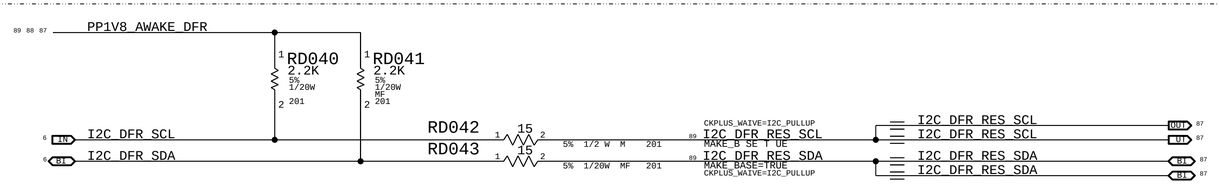
SIO I2C4

DIAGS BUS: 4

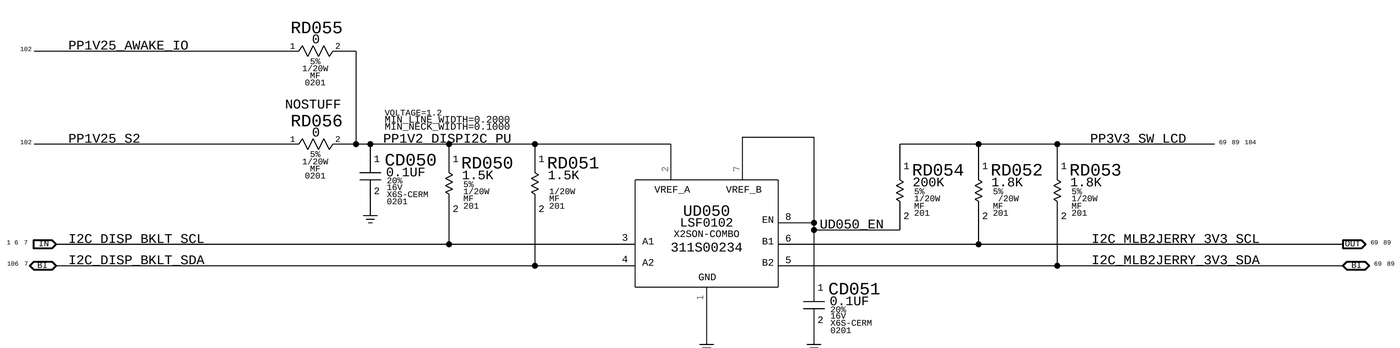
DEVICE	7-BIT
DFR DISPLAY	0X--
DFR TOUCH	0X--



DISP I2C

DIAGS BUS: 12

DEVICE	7-BIT
JERRY	0X--



BOM_COST_GROUP=SMC

SYNC_MASTER=T668_MLB SYNC_DATE=06/20/2019

PAGE TITLE

I2C: SIO, DISP

ISP I2C0

UNUSED

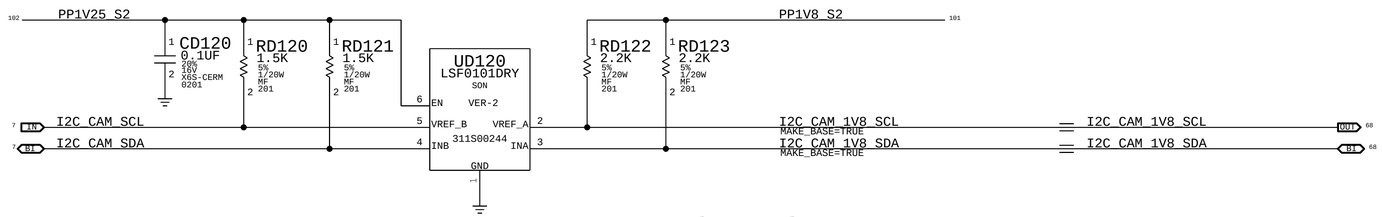
ISP I2C1

UNUSED

ISP I2C2

DIAGS BUS: TBD

DEVICE	7-BIT
CAMERA PMU	0X--
CAMERA SENSOR	0X--



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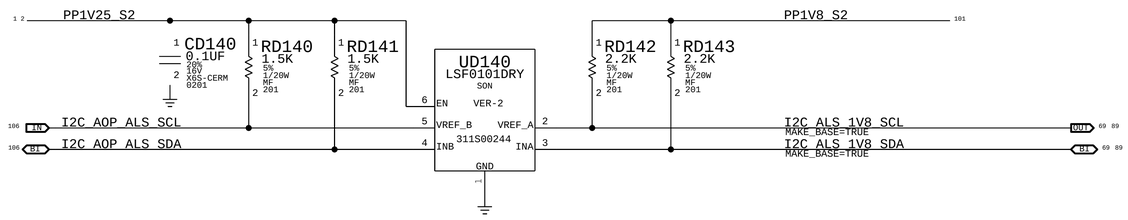
ISP I2C3

UNUSED

AOP I2C0

DIAGS BUS: 5

DEVICE	7-BIT
ALS CT720SW	0X29



AOP I2C1

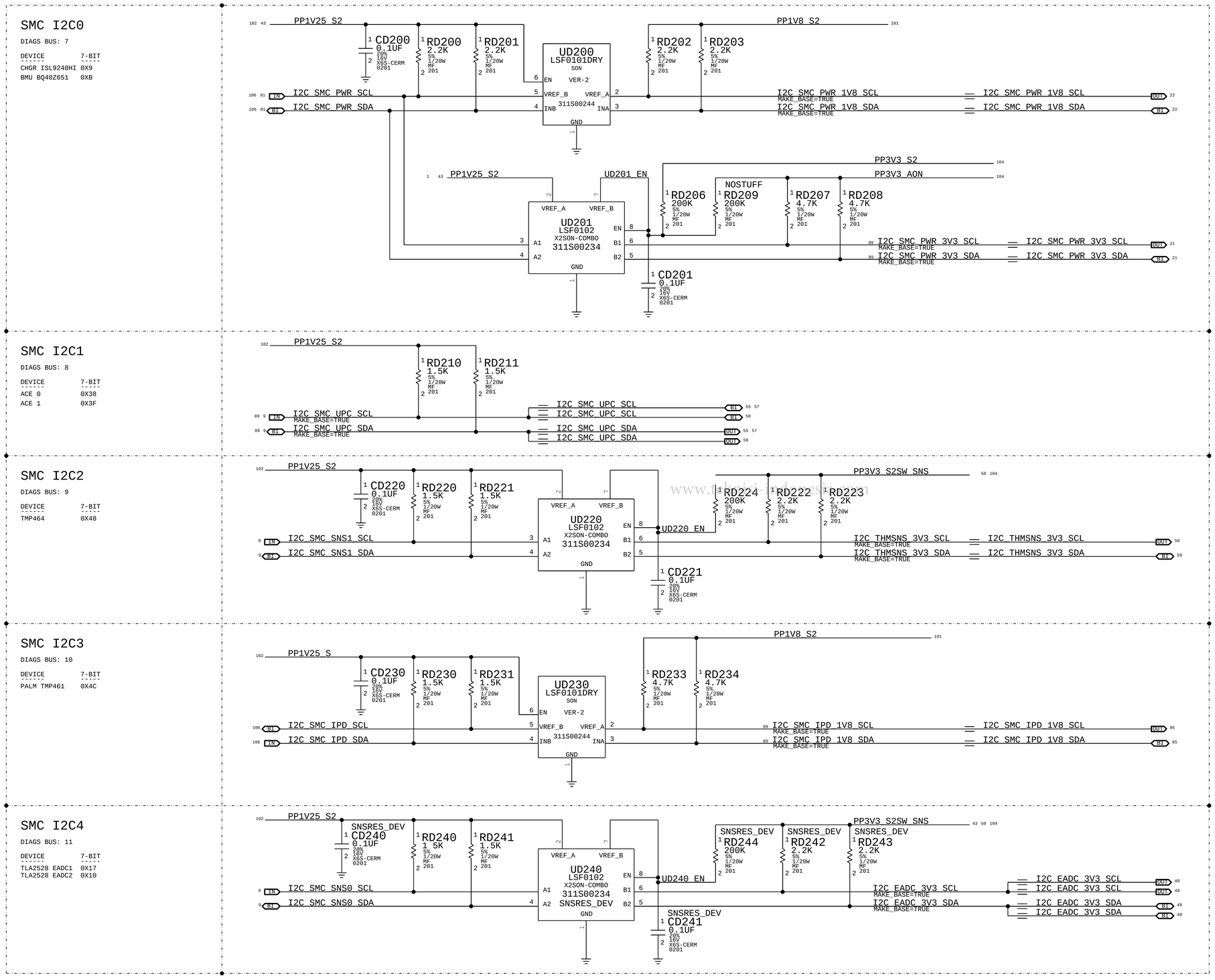
UNUSED

BOM_COST_GROUP=SMC

SYNC_MASTER=T668_MLB SYNC_DATE=06/20/2019

PAGE TITLE

I2C: ISP, AOP



BOM_COST_GROUP=SMC

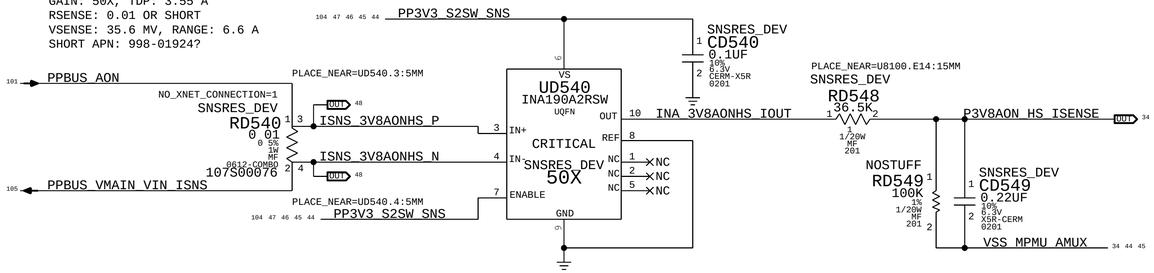
SYNC_MASTER=KEI_T668_MLB SYNC_DATE=12/20/2019

PAGE TITLE

I2C: SMC

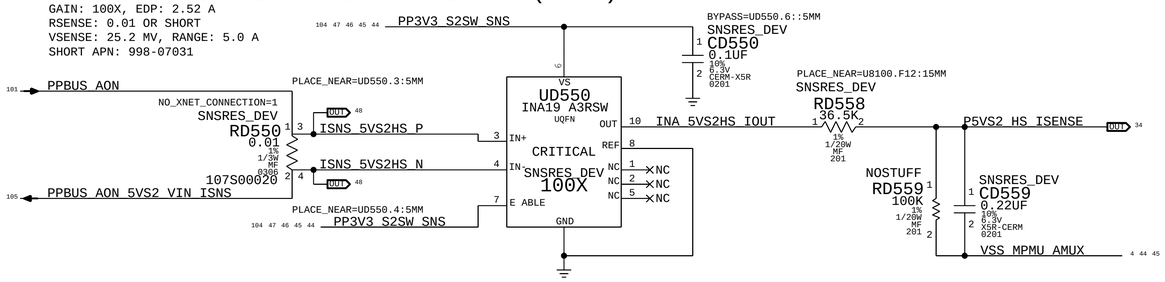
P3V8 AON HIGH SIDE CURRENT SENSE (IMVR)

GAIN: 50X, TDP: 3.55 A
RSENSE: 0.01 OR SHORT
VSENSE: 35.6 MV, RANGE: 6.6 A
SHORT APN: 998-01924?



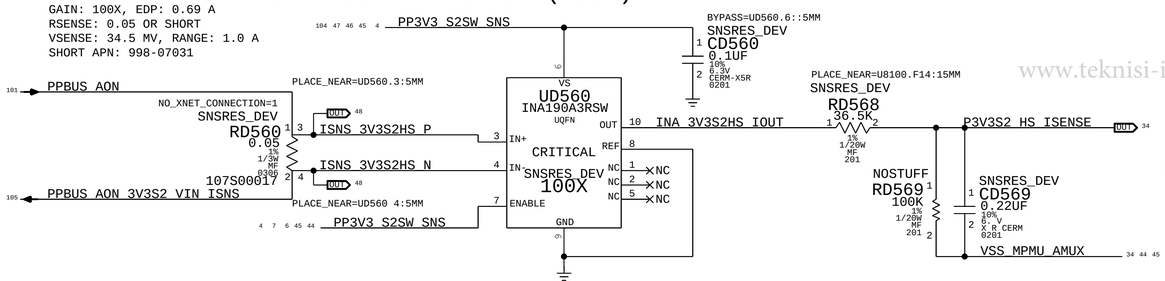
5V S2 VR HIGH SIDE CURRENT SENSE (IO5R)

GAIN: 100X, EDP: 2.52 A
RSENSE: 0.01 OR SHORT
VSENSE: 25.2 MV, RANGE: 5.0 A
SHORT APN: 998-07031



3V3 S2 VR HIGH SIDE CURRENT SENSE (IO3R)

GAIN: 100X, EDP: 0.69 A
RSENSE: 0.05 OR SHORT
VSENSE: 34.5 MV, RANGE: 1.0 A
SHORT APN: 998-07031



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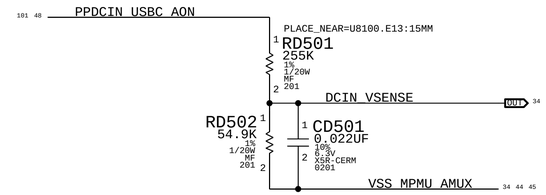
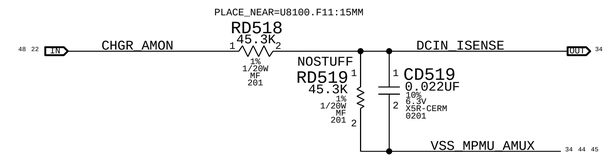
DCIN VOLTAGE SENSE (VD0R)

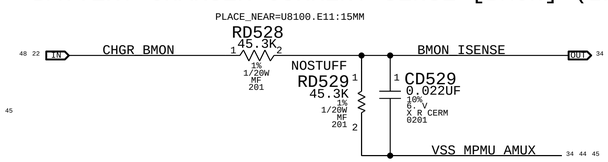
PMU AMUX inputs are not fail safe but RD501 limits the current rdar://60591705



DCIN CURRENT SENSE [AMON] (ID0R)

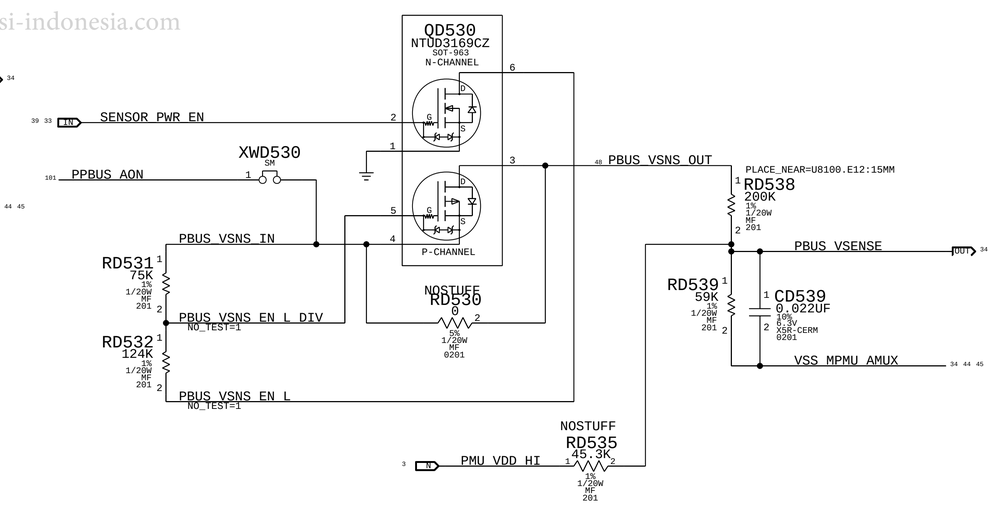


BATTERY CHARGER CURRENT SENSE [BMON] (IPBR)



PBUS VOLTAGE SENSE (VP0R)

RD531/RD532 updated per rdar://60591705

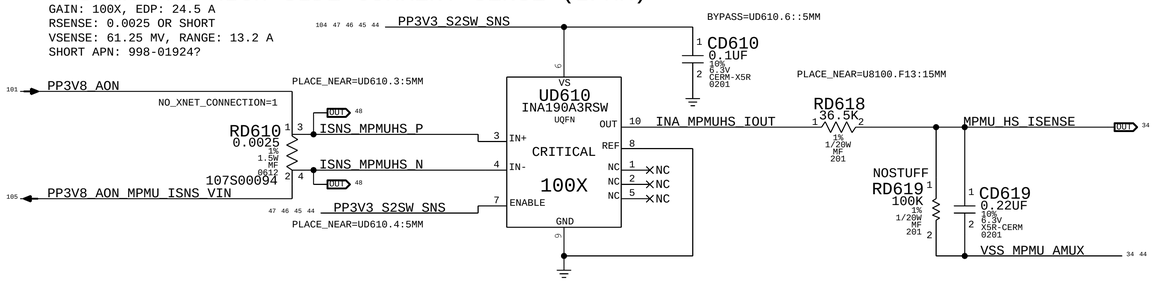


PAGE TITLE
SENSORS: POWER HIGH SIDE (1/2)

BOM_COST_GROUP=SENSORS

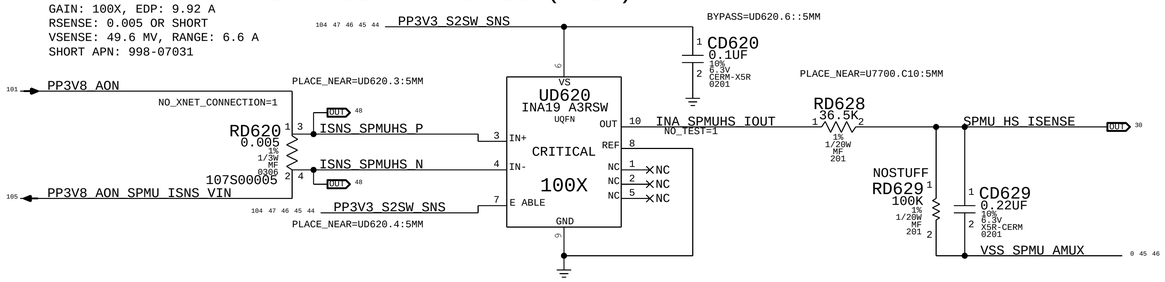
MASTER PMU HIGH SIDE CURRENT SENSE (IPMR)

GAIN: 100X, EDP: 24.5 A
RSENSE: 0.0025 OR SHORT
VSENSE: 61.25 MV, RANGE: 13.2 A
SHORT APN: 998-01924?



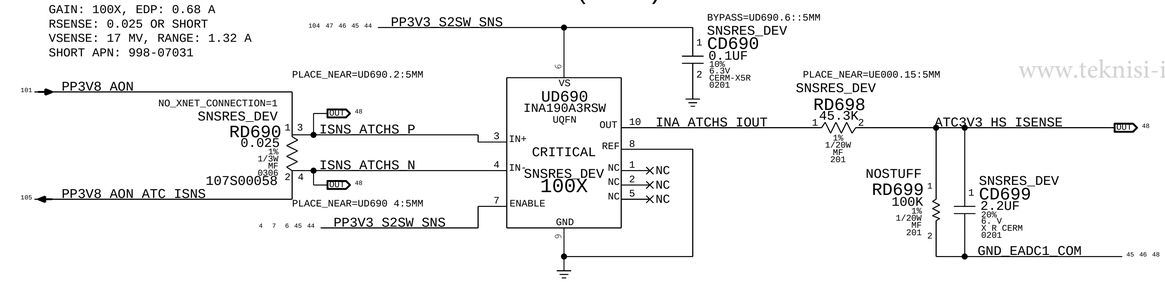
SLAVE PMU HIGH SIDE CURRENT SENSE (IPSR)

GAIN: 100X, EDP: 9.92 A
RSENSE: 0.005 OR SHORT
VSENSE: 49.6 MV, RANGE: 6.6 A
SHORT APN: 998-07031



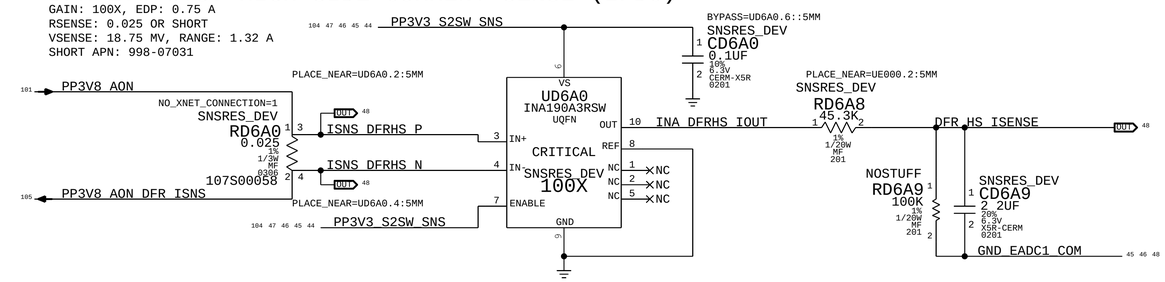
ATC 3V3 LDO HIGH SIDE CURRENT SENSE (IULR)

GAIN: 100X, EDP: 0.68 A
RSENSE: 0.025 OR SHORT
VSENSE: 17 MV, RANGE: 1.32 A
SHORT APN: 998-07031

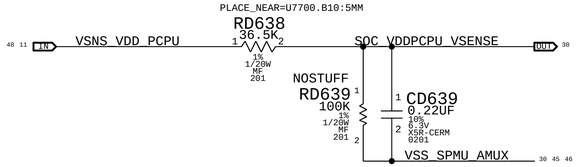


DFR 1.8/3.3V HIGH SIDE CURRENT SENSE (IFDC)

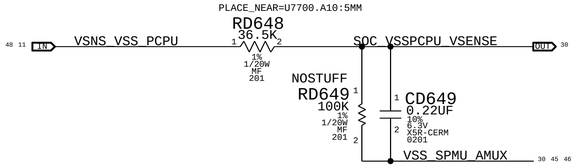
GAIN: 100X, EDP: 0.75 A
RSENSE: 0.025 OR SHORT
VSENSE: 18.75 MV, RANGE: 1.32 A
SHORT APN: 998-07031



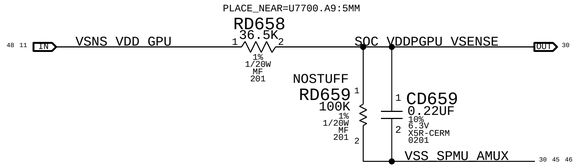
SOC VDD PCPU VSENSE (VCDP)



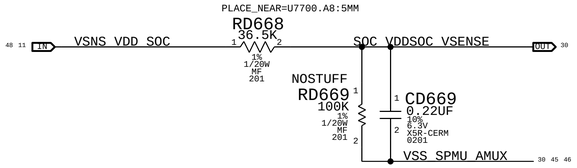
SOC VSS PCPU VSENSE (VCSP)



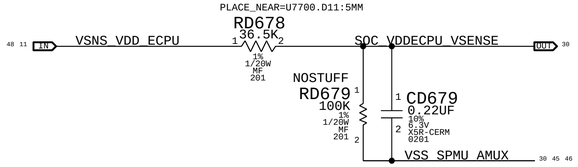
SOC VDD GPU VSENSE (VGDR)



SOC VDD SOC VSENSE (VSDR)

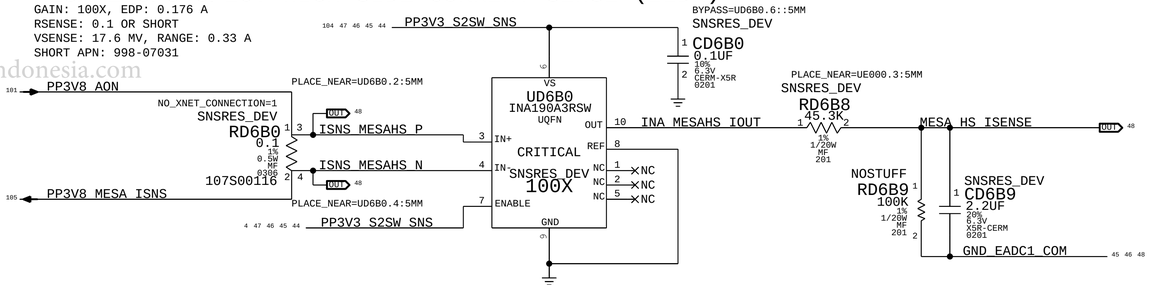


SOC VDD ECPU VSENSE (VCDE)



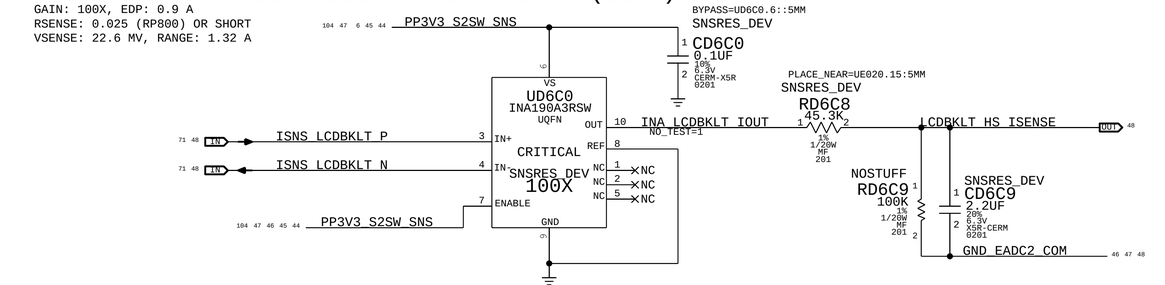
MESA 1.8/3.3/16V HIGH SIDE CURRENT SENSE (IIDR)

GAIN: 100X, EDP: 0.176 A
RSENSE: 0.1 OR SHORT
VSENSE: 17.6 MV, RANGE: 0.33 A
SHORT APN: 998-07031



LCD BACKLIGHT HIGH SIDE CURRENT SENSE (IBLR)

GAIN: 100X, EDP: 0.9 A
RSENSE: 0.025 (RP800) OR SHORT
VSENSE: 22.6 MV, RANGE: 1.32 A



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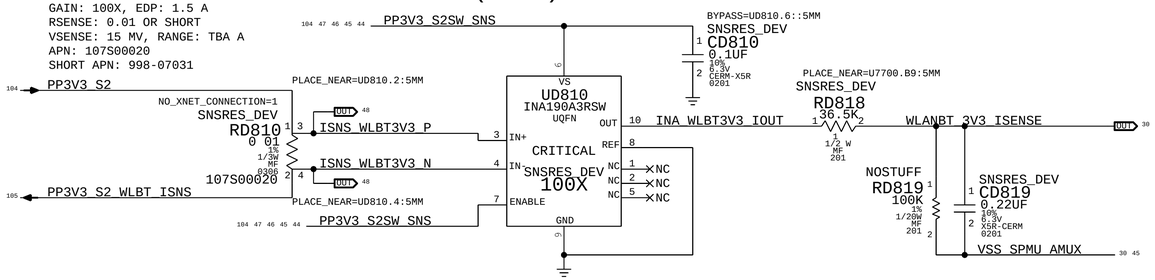
PAGE TITLE
SENSORS: POWER HIGH SIDE (2/2)

BOM_COST_GROUP=SENSORS

WLAN BT 3V3 S2 CURRENT SENSE (IW3C)

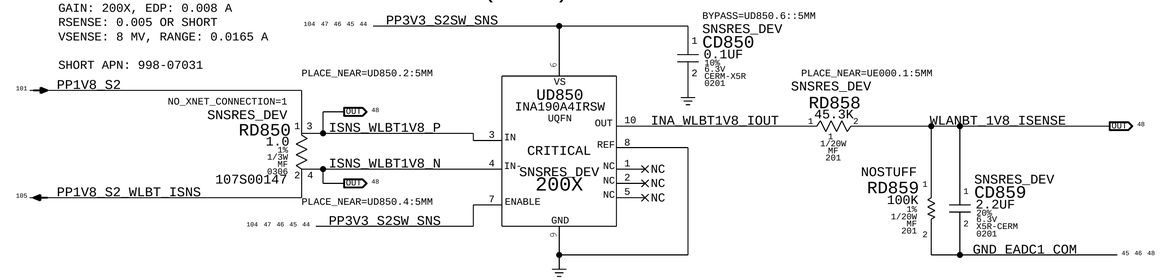
GAIN: 100X, EDP: 1.5 A
RSENSE: 0.01 OR SHORT
VSENSE: 15 MV, RANGE: TBA A
APN: 107S00020
SHORT APN: 998-07031



WLAN BT 1V8 S2 CURRENT SENSE (IW2C)

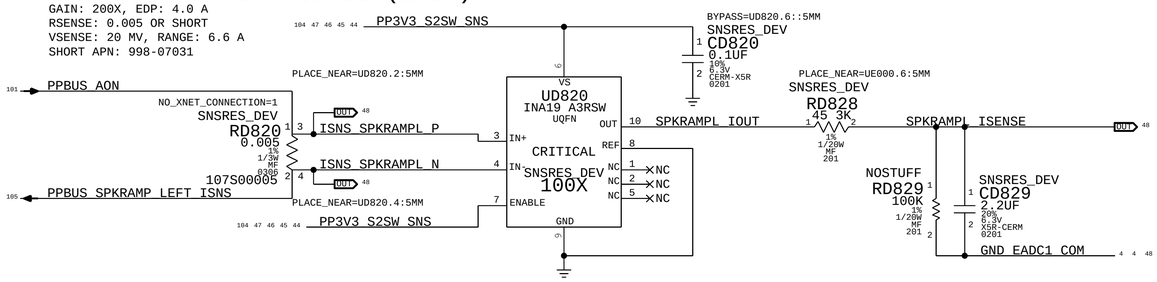
GAIN: 200X, EDP: 0.008 A
RSENSE: 0.005 OR SHORT
VSENSE: 8 MV, RANGE: 0.0165 A

SHORT APN: 998-07031



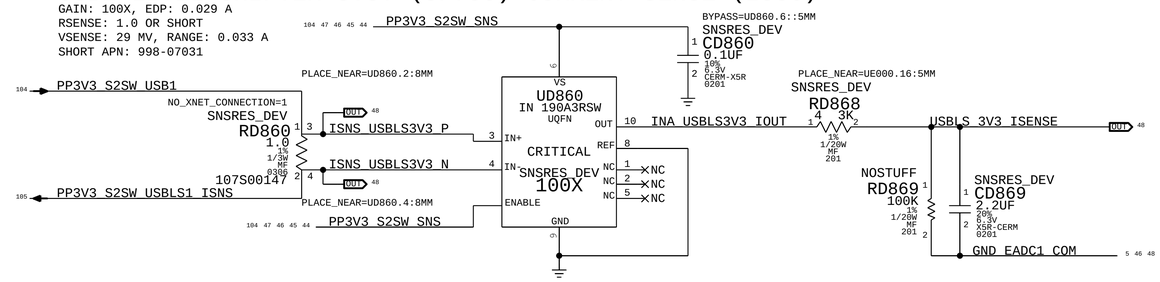
LEFT AMP CURRENT SENSE (IALR)

GAIN: 200X, EDP: 4.0 A
RSENSE: 0.005 OR SHORT
VSENSE: 20 MV, RANGE: 6.6 A
SHORT APN: 998-07031



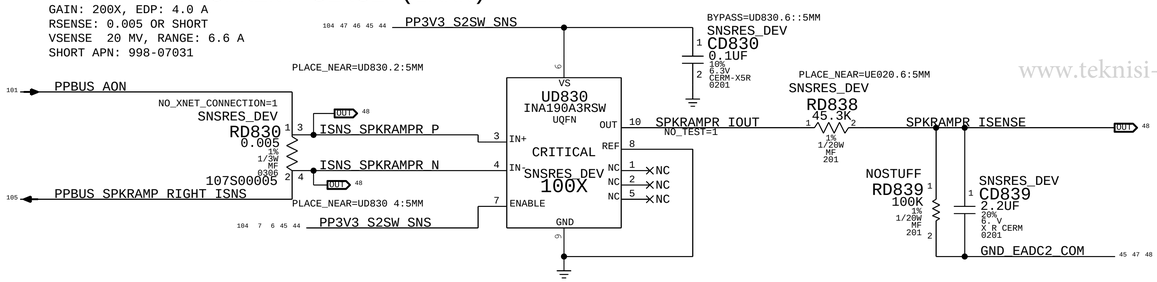
USB2 LEVEL SHIFTER 3.3V (UF750) CURRENT SENSE (IU3C)

GAIN: 100X, EDP: 0.029 A
RSENSE: 1.0 OR SHORT
VSENSE: 29 MV, RANGE: 0.033 A
SHORT APN: 998-07031



RIGHT AMP CURRENT SENSE (IARR)

GAIN: 200X, EDP: 4.0 A
RSENSE: 0.005 OR SHORT
VSENSE 20 MV, RANGE: 6.6 A
SHORT APN: 998-07031



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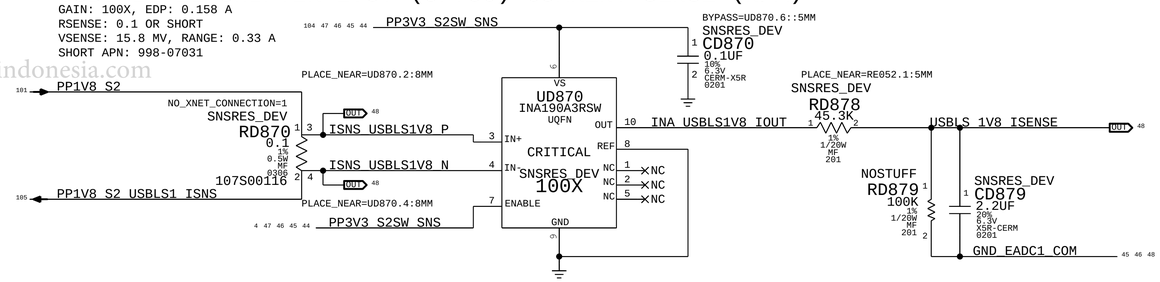
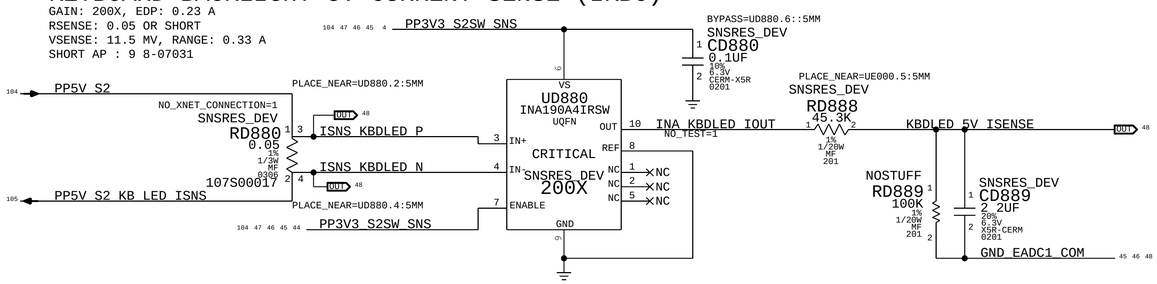
USB2 LEVEL SHIFTER 1.8V (UF750) CURRENT SENSE (N/A)

GAIN: 100X, EDP: 0.158 A
RSENSE: 0.1 OR SHORT
VSENSE: 15.8 MV, RANGE: 0.33 A
SHORT APN: 998-07031



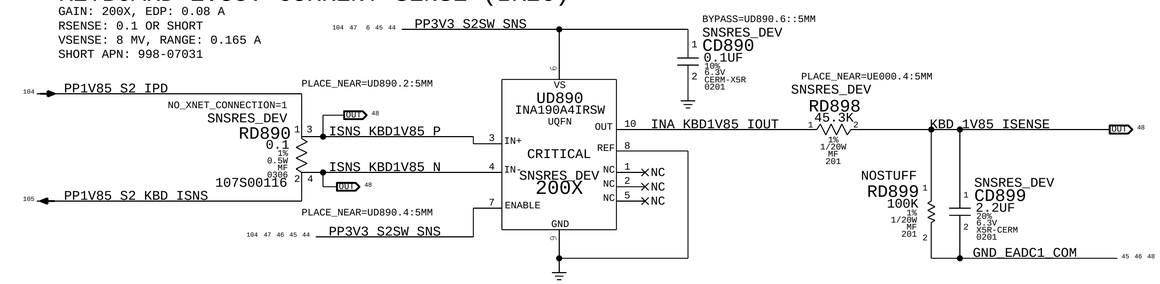
KEYBOARD BACKLIGHT 5V CURRENT SENSE (IKBC)

GAIN: 200X, EDP: 0.23 A
RSENSE: 0.05 OR SHORT
VSENSE: 11.5 MV, RANGE: 0.33 A
SHORT AP : 9 8-07031



KEYBOARD 1.85V CURRENT SENSE (IK2C)

GAIN: 200X, EDP: 0.08 A
RSENSE: 0.1 OR SHORT
VSENSE: 8 MV, RANGE: 0.165 A
SHORT APN: 998-07031



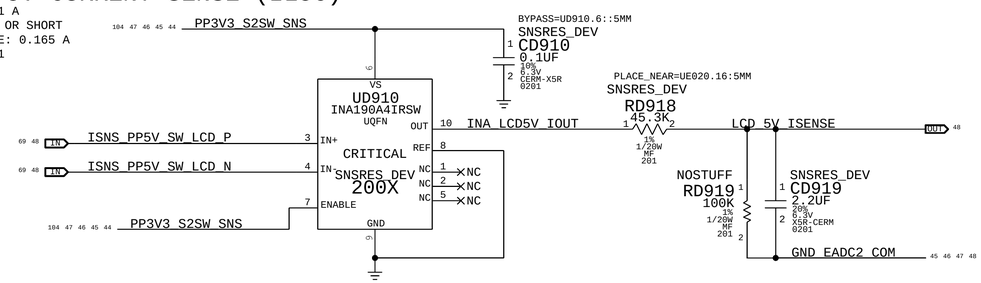
PAGE TITLE
SENSORS: POWER LOW SIDE (1/2)

BOM_COST_GROUP=SENSORS

TODO: UPDATE PLACE NEAR

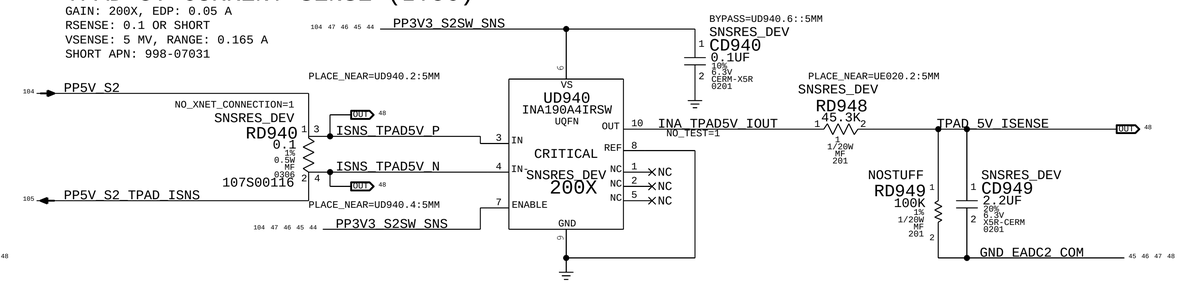
LCD PANEL 5V CURRENT SENSE (IL5C)

GAIN: 200X, EDP: 0.1 A
RSENSE: 0.1 (RP621) OR SHORT
VSENSE: 10 MV, RANGE: 0.165 A
SHORT APN: 998-07031



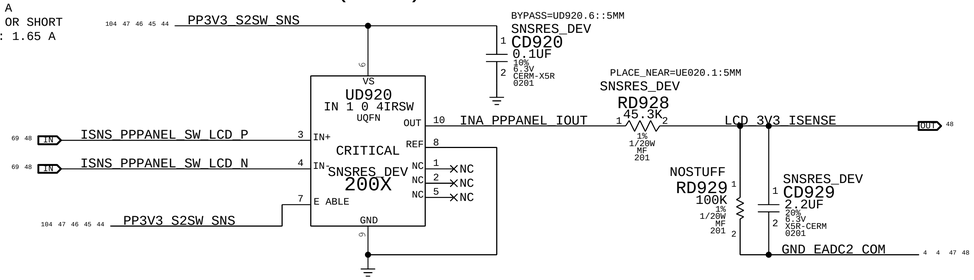
TPAD 5V CURRENT SENSE (IT5C)

GAIN: 200X, EDP: 0.05 A
RSENSE: 0.1 OR SHORT
VSENSE: 5 MV, RANGE: 0.165 A
SHORT APN: 998-07031



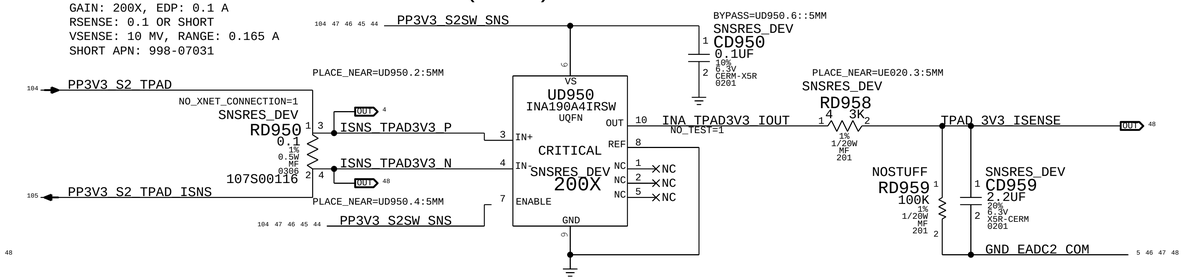
LCD PANEL 3.3/3.8V CURRENT SENSE (IL3C)

GAIN: 200X, EDP: 1.0 A
RSENSE: 0.01 (RP620) OR SHORT
VSENSE: 10 MV, RANGE: 1.65 A
SHORT APN: 998-07031



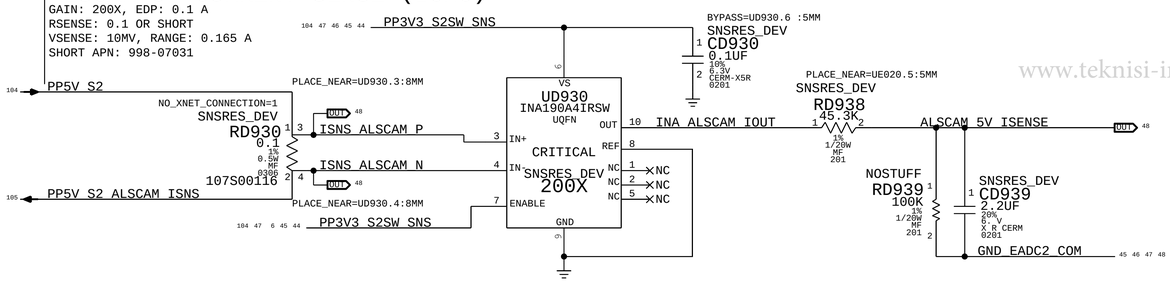
TPAD 3.3V S2 CURRENT SENSE (IT3C)

GAIN: 200X, EDP: 0.1 A
RSENSE: 0.1 OR SHORT
VSENSE: 10 MV, RANGE: 0.165 A
SHORT APN: 998-07031



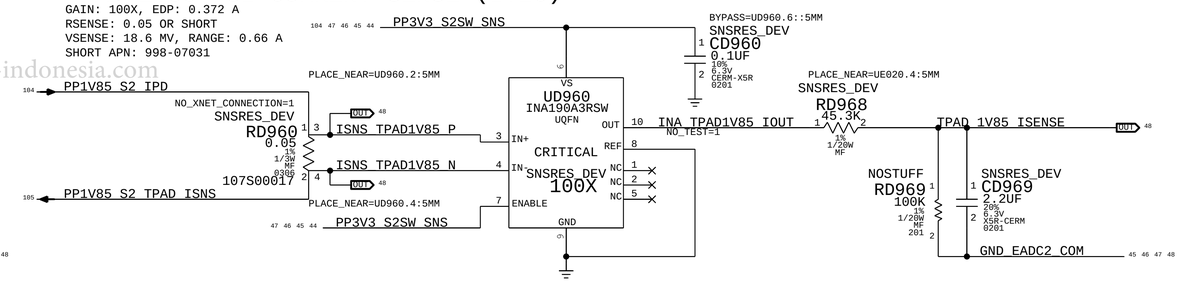
ALSCAM 5V CURRENT SENSE (ICMC)

GAIN: 200X, EDP: 0.1 A
RSENSE: 0.1 OR SHORT
VSENSE: 10MV, RANGE: 0.165 A
SHORT APN: 998-07031



TPAD 1.85V S2 CURRENT SENSE (IT2C)

GAIN: 100X, EDP: 0.372 A
RSENSE: 0.05 OR SHORT
VSENSE: 18.6 MV, RANGE: 0.66 A
SHORT APN: 998-07031



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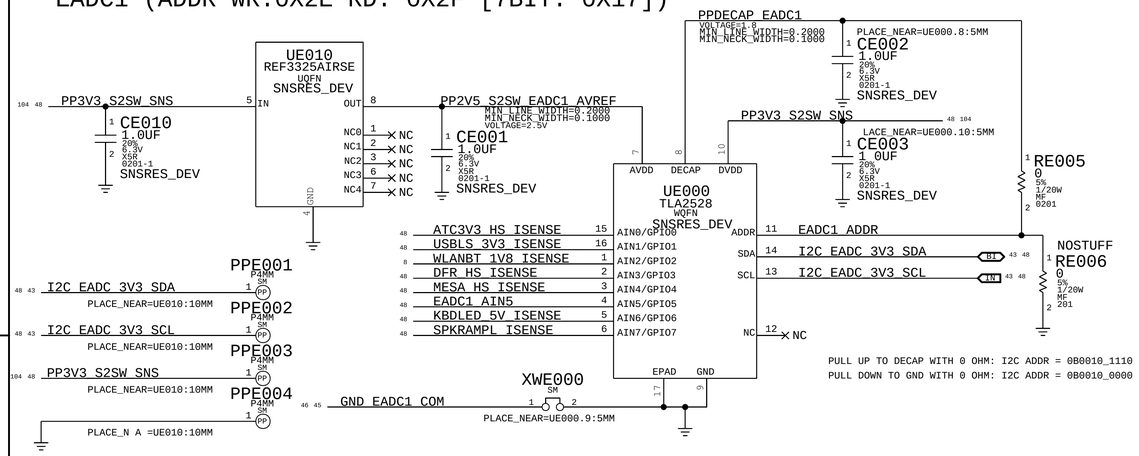
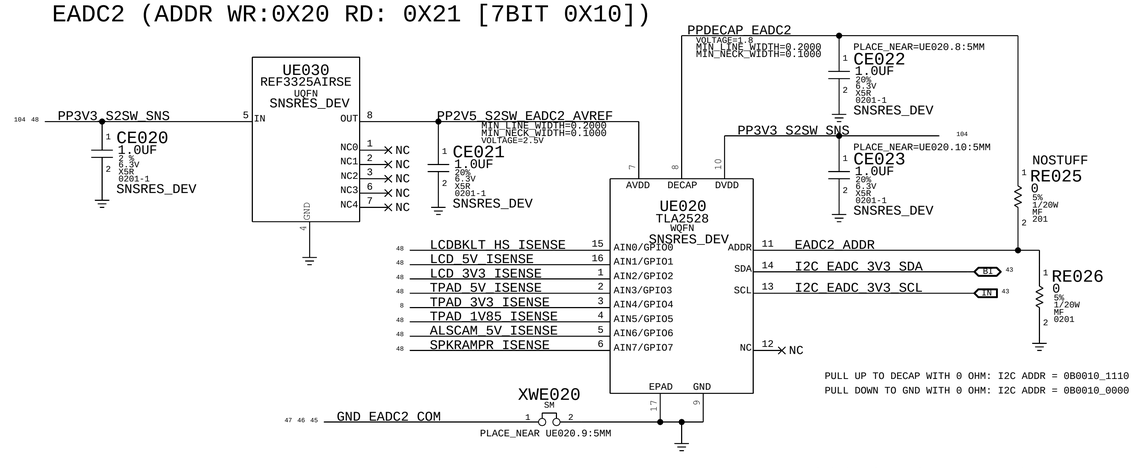
BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: POWER LOW SIDE (2/2)

EADC1 (ADDR WR:0X2E RD: 0X2F [7BIT: 0X17])



EADC2 (ADDR WR:0X20 RD: 0X21 [7BIT 0X10])



EADC1 AIN ALIAS

ATC3V3_HS_ISENSE	MAKE_BASE=TRUE NO_TEST=1	ATC3V3_HS_ISENSE
USBLS_3V3_ISENSE	MAKE_BASE=TRUE	USBLS_3V3_ISENSE
WLANBT_1V8_ISENSE	MAKE_BASE=TRUE NO_TEST=1	WLANBT_1V8_ISENSE
DFR_HS_ISENSE	MAKE_BASE=TRUE NO_TEST=1	DFR_HS_ISENSE
MESA_HS_ISENSE	MAKE_BASE=TRUE NO_TEST=1	MESA_HS_ISENSE
KBDLED_5V_ISENSE	MAKE_BASE=TRUE NO_TEST=1	KBDLED_5V_ISENSE
SPKRAMPL_ISENSE	MAKE_BASE=TRUE NO_TEST=1	SPKRAMPL_ISENSE

PLACE_NEAR=UE000.4:5MM
RE051 0 1/20W 5% MF 0201
KBD_1V85_ISENSE NO_TEST=1 — EADC1_AIN5 NO_TEST=1

PLACE_NEAR=UE000.4:5MM
RE052 0 1/20W 5% MF 0201 NOSTUFF
USBLS_1V8_ISENSE NO_TEST=1

EADC2 AIN ALIAS

LCDBKLT_HS_ISENSE	MAKE_BASE=TRUE NO_TEST=1	LCDBKLT_HS_ISENSE
LCD_5V_ISENSE	MAKE_BASE=TRUE NO_TEST=1	LCD_5V_ISENSE
LCD_3V3_ISENSE	MAKE_BASE=TRUE NO_TEST=1	LCD_3V3_ISENSE
TPAD_5V_ISENSE	MAKE_BASE=TRUE NO_TEST=1	TPAD_5V_ISENSE
TPAD_3V3_ISENSE	MAKE_BASE=TRUE NO_TEST=1	TPAD_3V3_ISENSE
TPAD_1V85_ISENSE	MAKE_BASE=TRUE NO_TEST=1	TPAD_1V85_ISENSE
ALSCAM_5V_ISENSE	MAKE_BASE=TRUE NO_TEST=1	ALSCAM_5V_ISENSE
SPKRAMPR_ISENSE	MAKE_BASE=TRUE NO_TEST=1	SPKRAMPR_ISENSE

POWER VALIDATION TEST POINTS (WIP)

ISNS_3V8AONHS_P	TPE001	PLACE_SIDE=TOP PLACE_NEAR=RD540.3:5MM
ISNS_3V8AONHS_N	TPE002	PLACE_SIDE=TOP PLACE_NEAR=RD540.4:5MM
ISNS_5VS2HS_P	TPE003	PLACE_SIDE=TOP PLACE_NEAR=RD550.3:5MM
ISNS_5VS2HS_N	TPE004	PLACE_SIDE=TOP PLACE_NEAR=RD550.4:5MM
ISNS_3V3S2HS_P	TPE005	PLACE_SIDE=TOP PLACE_NEAR=RD560.3:5MM
ISNS_3V3S2HS_N	TPE006	PLACE_SIDE=TOP PLACE_NEAR=RD560.4:5MM
PPDCIN_USBC_AON	TPE007	PLACE_SIDE=TOP PLACE_NEAR=RD501.1:5MM
	TPE008	PLACE_SIDE=TOP PLACE_NEAR=RD502.2:5MM
CHGR_AMON	TPE009	PLACE_SIDE=TOP
	TPE010	PLACE_SIDE=TOP PLACE_NEAR=TPE009.1:5MM
CHGR_BMON	TPE011	PLACE_SIDE=TOP
	TPE012	PLACE_SIDE=TOP PLACE_NEAR=TPE011.1:5MM
PBUS_VSNS_OUT	TPE013	PLACE_SIDE=TOP PLACE_NEAR=RD538.1:10MM
	TPE014	PLACE_SIDE=TOP PLACE_NEAR=TPE013.1:5MM
ISNS_MPMUHS_P	TPE015	PLACE_SIDE=TOP PLACE_NEAR=RD610.3:10MM
ISNS_MPMUHS_N	TPE016	PLACE_SIDE=TOP PLACE_NEAR=RD610.4:10MM
ISNS_SPMUHS_P	TPE017	PLACE_SIDE=TOP PLACE_NEAR=RD620.3:5MM
ISNS_SPMUHS_N	TPE018	PLACE_SIDE=TOP PLACE_NEAR=RD620.4:5MM
ISNS_ATCHS_P	TPE019	PLACE_SIDE=TOP PLACE_NEAR=RD690.3:5MM
ISNS_ATCHS_N	TPE020	PLACE_SIDE=TOP PLACE_NEAR=RD690.4:5MM
ISNS_DFRHS_P	TPE021	PLACE_SIDE=TOP PLACE_NEAR=RD6A0.3:10MM
ISNS_DFRHS_N	TPE022	PLACE_SIDE=TOP PLACE_NEAR=RD6A0.4:10MM
ISNS_MESAHS_P	TPE023	PLACE_SIDE=TOP PLACE_NEAR=RD6B0.3:5MM
ISNS_MESAHS_N	TPE024	PLACE_SIDE=TOP PLACE_NEAR=RD6B0.4:5MM
ISNS_LCDBKLT_P	TPE025	PLACE_SIDE=TOP PLACE_NEAR=RP800.4:5MM
ISNS_LCDBKLT_N	TPE026	PLACE_SIDE=TOP PLACE_NEAR=RP800.3:5MM
ISNS_WLBT3V3_P	TPE027	PLACE_SIDE=TOP PLACE_NEAR=RD810.3:5MM
ISNS_WLBT3V3_N	TPE028	PLACE_SIDE=TOP PLACE_NEAR=RD810.4:5MM
ISNS_SPKRAMPL_P	TPE029	PLACE_SIDE=TOP PLACE_NEAR=RD820.3:5MM
ISNS_SPKRAMPL_N	TPE030	PLACE_SIDE=TOP PLACE_NEAR=RD820.4:5MM
ISNS_SPKRAMPR_P	TPE031	PLACE_SIDE=TOP PLACE_NEAR=RD830.3:5MM
ISNS_SPKRAMPR_N	TPE032	PLACE_SIDE=TOP PLACE_NEAR=RD830.4:5MM
ISNS_KBDLED_P	TPE033	PLACE_SIDE=TOP PLACE_NEAR=RD880.3:5MM
ISNS_KBDLED_N	TPE034	PLACE_SIDE=TOP PLACE_NEAR=RD880.4:5MM
ISNS_WLBT1V8_P	TPE035	PLACE_SIDE=TOP PLACE_NEAR=RD850.3:5MM
ISNS_WLBT1V8_N	TPE036	PLACE_SIDE=TOP PLACE_NEAR=RD850.4:5MM
ISNS_USBLS3V3_P	TPE037	PLACE_SIDE=TOP PLACE_NEAR=RD860.3:10MM
ISNS_USBLS3V3_N	TPE038	PLACE_SIDE=TOP PLACE_NEAR=RD860.4:10MM
ISNS_USBLS1V8_P	TPE039	PLACE_SIDE=TOP PLACE_NEAR=RD870.4:10MM
ISNS_USBLS1V8_N	TPE040	PLACE_SIDE=TOP PLACE_NEAR=RD870.3:10MM
ISNS_KBD1V85_P	TPE041	PLACE_SIDE=TOP PLACE_NEAR=RD890.3:10MM
ISNS_KBD1V85_N	TPE042	PLACE_SIDE=TOP PLACE_NEAR=RD890.4:10MM
ISNS_PP5V_SW_LCD_P	TPE043	PLACE_SIDE=TOP PLACE_NEAR=RP621.3:5MM
ISNS_PP5V_SW_LCD_N	TPE044	PLACE_SIDE=TOP PLACE_NEAR=RP621.4:5MM
ISNS_PPPANEL_SW_LCD_P	TPE045	PLACE_SIDE=TOP PLACE_NEAR=RP620.3:5MM
ISNS_PPPANEL_SW_LCD_N	TPE046	PLACE_SIDE=TOP PLACE_NEAR=RP620.4:5MM
ISNS_ALSCAM_P	TPE047	PLACE_SIDE=TOP PLACE_NEAR=RD930.3:5MM
ISNS_ALSCAM_N	TPE048	PLACE_SIDE=TOP PLACE_NEAR=RD930.4:5MM
ISNS_TPAD5V_P	TPE049	PLACE_SIDE=TOP PLACE_NEAR=RD940.3:5MM
ISNS_TPAD5V_N	TPE050	PLACE_SIDE=TOP PLACE_NEAR=RD940.4:5MM
ISNS_TPAD3V3_P	TPE051	PLACE_SIDE=TOP PLACE_NEAR=RD950.3:10MM
ISNS_TPAD3V3_N	TPE052	PLACE_SIDE=TOP PLACE_NEAR=RD950.4:10MM
ISNS_TPAD1V85_P	TPE053	PLACE_SIDE=TOP PLACE_NEAR=RD960.3:5MM
ISNS_TPAD1V85_N	TPE054	PLACE_SIDE=TOP PLACE_NEAR=RD960.4:5MM
CHGR_CSI_P	TPE055	PLACE_SIDE=TOP PLACE_NEAR=R5220.3:15MM
CHGR_CSI_N	TPE056	PLACE_SIDE=TOP PLACE_NEAR=R5220.4:15MM
CHGR_CSO_P	TPE057	PLACE_SIDE=TOP
CHGR_CSO_N	TPE058	PLACE_SIDE=TOP PLACE_NEAR=TPE057.1:5MM

PROBE POINTS

PPVDD_CPU_SRAM_AWAKE	PPE0B1	PLACE_SIDE=TOP
PP0V764_S1_SRAM	PPE0B2	PLACE_SIDE=TOP
PP0V72_S2_VDD_LOW	PPE0B3	PLACE_SIDE=TOP

SOC SENSE LINES

VSNS_VDD_PCPU	PPE0A1	PLACE_SIDE=TOP
VSNS_VSS_PCPU	PPE0A2	PLACE_SIDE=TOP
VSNS_VDD_GPU NO_TEST=1	PPE0A3	PLACE_SIDE=TOP
VSNS_VDD_SOC NO_TEST=1	PPE0A4	PLACE_SIDE=TOP
VSNS_VDD_ECPU	PPE0A5	PLACE_SIDE=TOP
VSNS_VDD_DISP NO_TEST=1	PPE0A6	PLACE_SIDE=TOP
VSNS_VDD2_1 NO_TEST=1	PPE0A7	PLACE_SIDE=TOP
VSNS_VSS_1 NO_TEST=1	PPE0A8	PLACE_SIDE=TOP
VSNS_VDD2_2	PPE0A9	PLACE_SIDE=TOP
VSNS_VSS_2	PPE0AA	PLACE_SIDE=TOP
VSNS_VDD_DCS NO_TEST=1	PPE0AB	PLACE_SIDE=TOP
VSNS_VSS_DDR NO_TEST=1	PPE0AC	PLACE_SIDE=TOP
VSNS_VDDQL NO_TEST=1	PPE0AD	PLACE_SIDE=TOP
	PPE0AE	PLACE_NEAR=PPE0A3:2MM PLACE_SIDE=TOP
	PPE0AF	PLACE_SIDE=TOP

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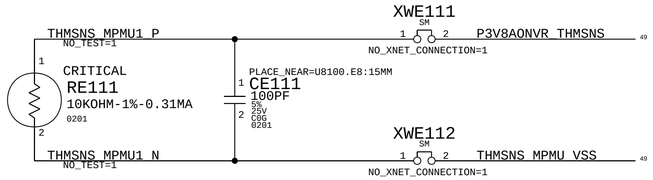
PAGE TITLE
SENSORS: POWER SUPPORT

BOM_COST_GROUP=SENSORS

8 | 7 | 2 | 1

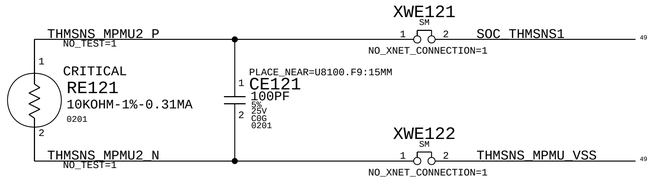
MASTER PMU TDEV1 [TMVR]

LOCATION: 3.8V AON VR BETWEEN PHASE 2 AND PHASE3 MOSFETS



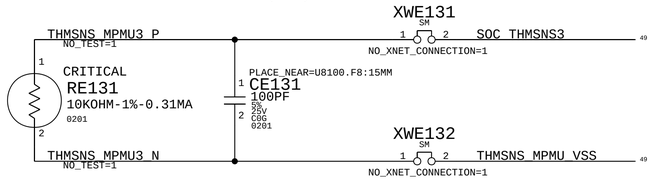
MASTER PMU TDEV2 [TSDD]

LOCATION: SOC DRAM AREA, BACKSIDE (TOP)



MASTER PMU TDEV3 [TSCD]

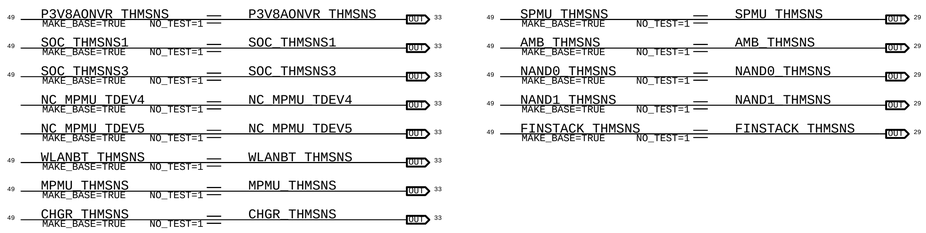
LOCATION: SOC CORE AREA BACKSIDE (TOP)



MASTER PMU TDEV4 & TDEV5

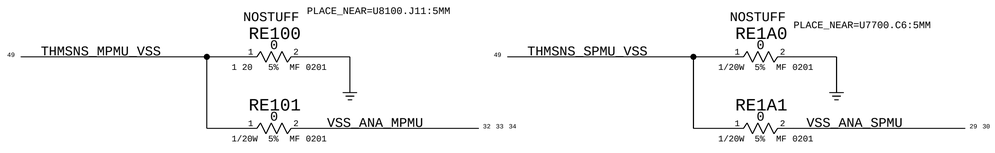
LOCATION: DOES NOT EXIST

PMU TDEV MAPPING



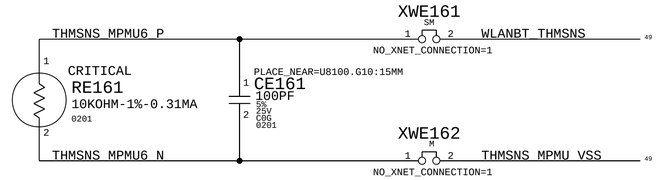
TAP NEGATIVE CLOSE TO VSS_REF

ADDED OPTION PER RDAR://60203428



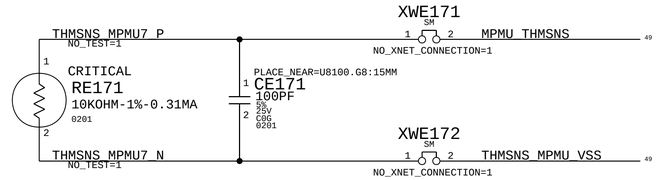
MASTER PMU TDEV6 [TW0P]

LOCATION: WLANBT, BACKSIDE



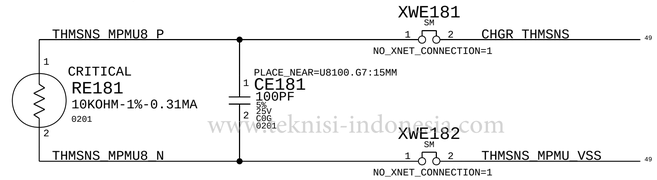
MASTER PMU TDEV7 [TPMP]

LOCATION: MASTER PMU, BETWEEN BUCK0 AND BUCK1 INDUCTORS



MASTER PMU TDEV8 [TCHP]

LOCATION: CHARGER, BETWEEN INDUCTOR AND MOSFETS



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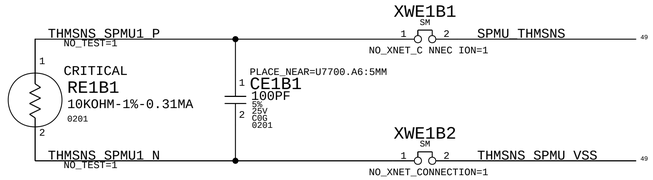
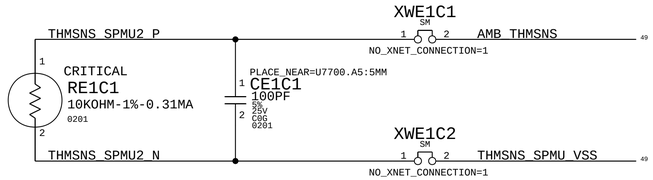
SLAVE PMU TDEV1 [TPSP]

LOCATION: SLAVE PMU, BUCK10 INDUCTOR PROXIMITY



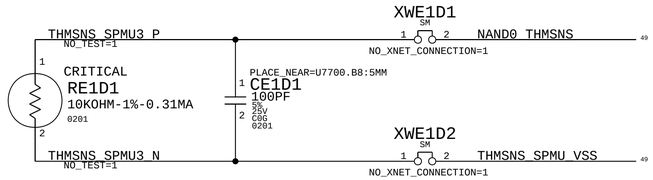
SLAVE PMU TDEV2 [TaMP]

LOCATION: MLB AIR INTAKE PROXIMITY



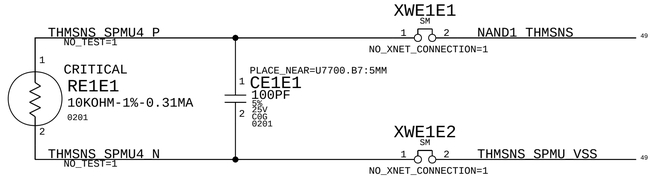
SLAVE PMU TDEV3 [TH0T]

LOCATION: LOWER LEFT CORNER OF NAND DEVICES



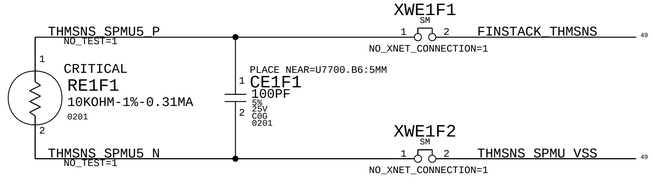
SLAVE PMU TDEV4 [TH0B]

LOCATION: UPPER RIGHT CORNER OF NAND DEVICES



SLAVE PMU TDEV5 [Th1H]

LOCATION: FINSTACK PROXIMITY



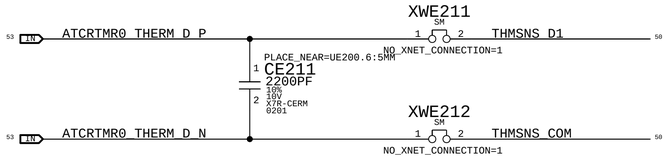
BOM_COST_GROUP=SENSORS

PAGE TITLE

SENSORS: THERMAL (1/2)

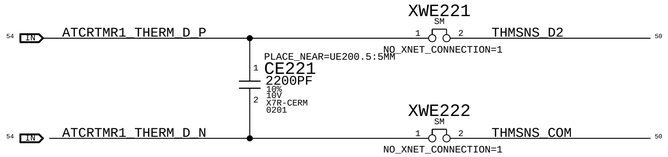
RETIMER ATC0 [TT0D]

LOCATION: ON CHIP



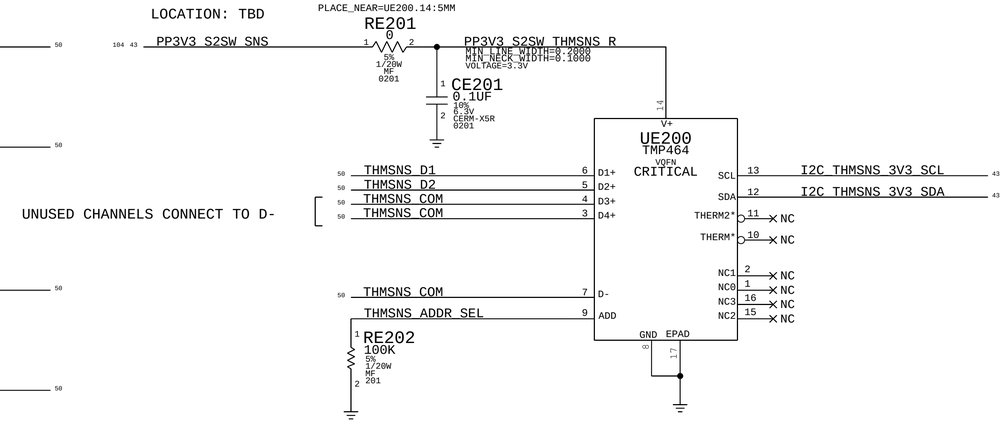
RETIMER ATC1 [TT1D]

LOCATION: ON CHIP



I/O PROXIMITY [TIOP]
I2C ADDR WR:0X90 RD: 0X91

LOCATION: TBD



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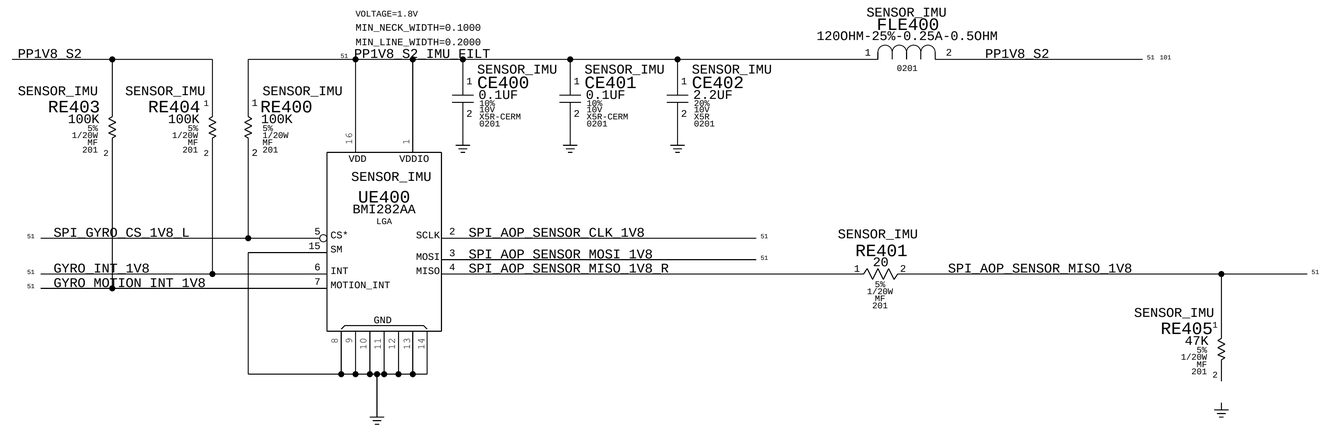
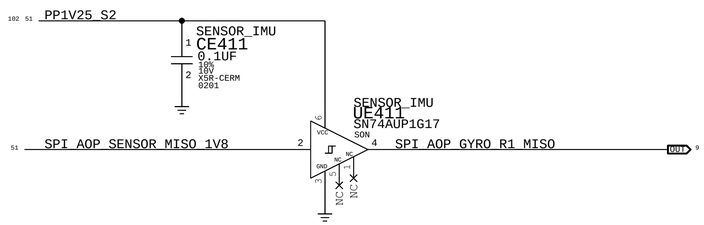
PAGE TITLE

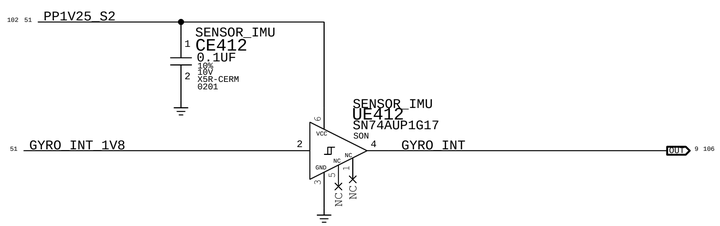
SENSORS: THERMAL (2/2)

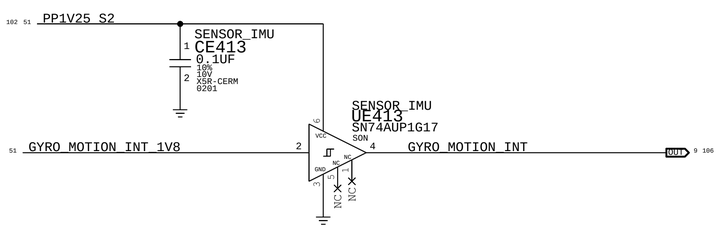
BOM_COST_GROUP=SENSORS

KOBOL: ACCEL & GYRO

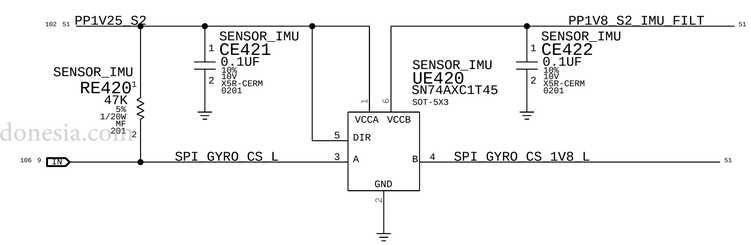








SPI LEVEL TRANSLATION



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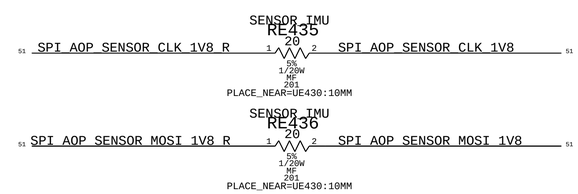
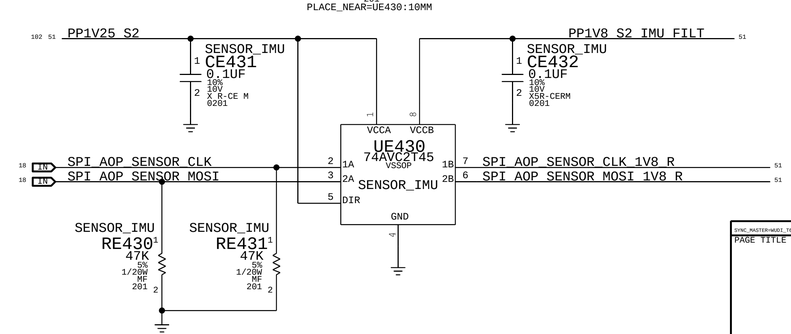




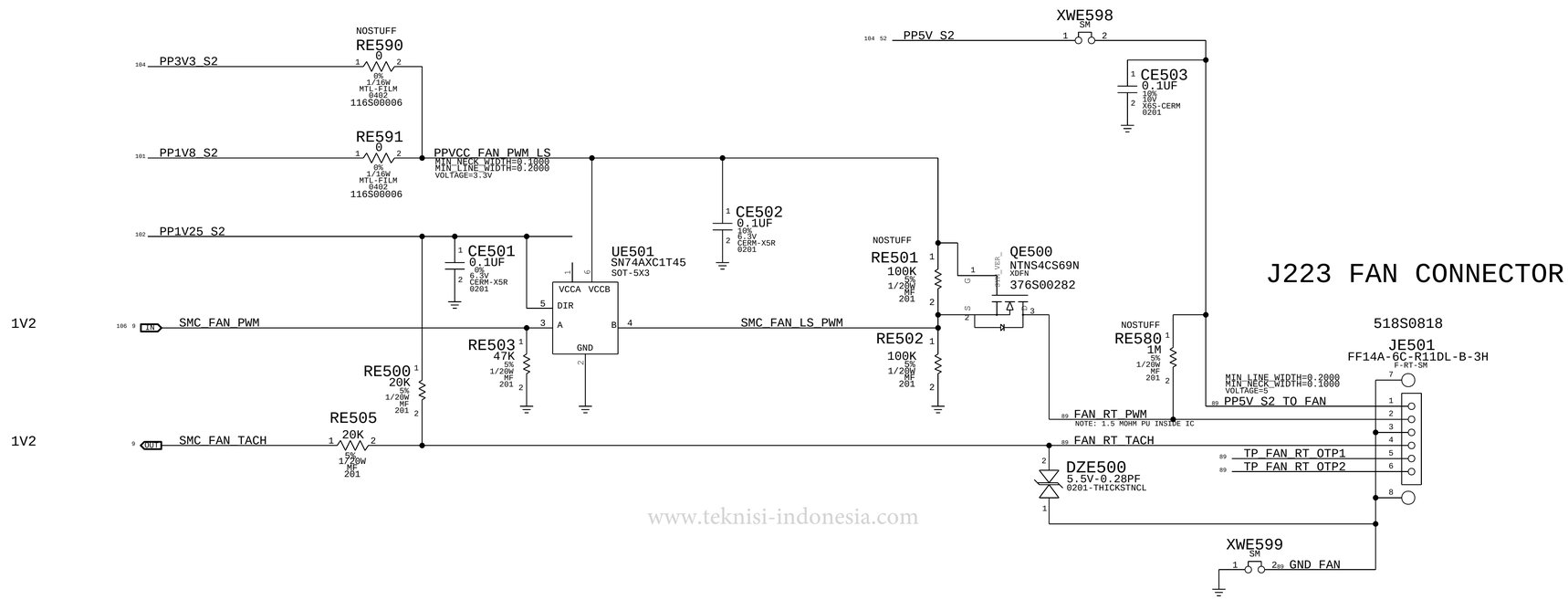
BOM_COST_GROUP=SENSORS

SYNC_MASTER=WADI_T668_MLB

PAGE TITLE

SENSORS: MOTION

FAN CONTROL



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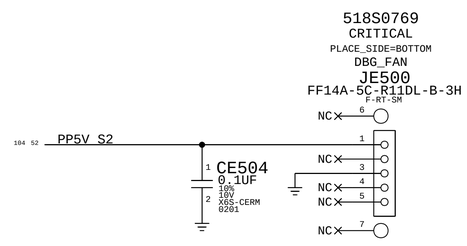
5V POWER FOR A DEBUG FAN



BOM_COST_GROUP=FAN

SYNC_MASTER=AITKEN_T668_MLB SYNC_DATE=09/18/2019

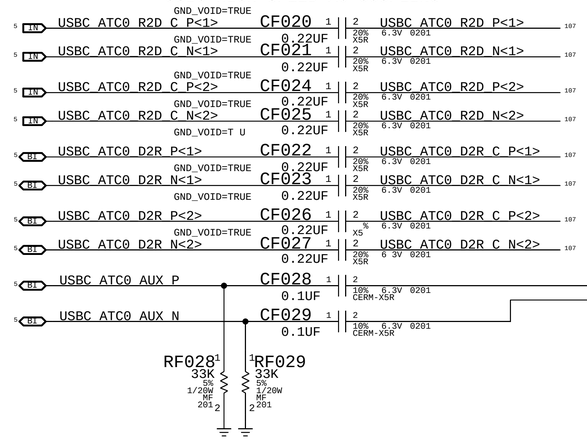
PAGE TITLE

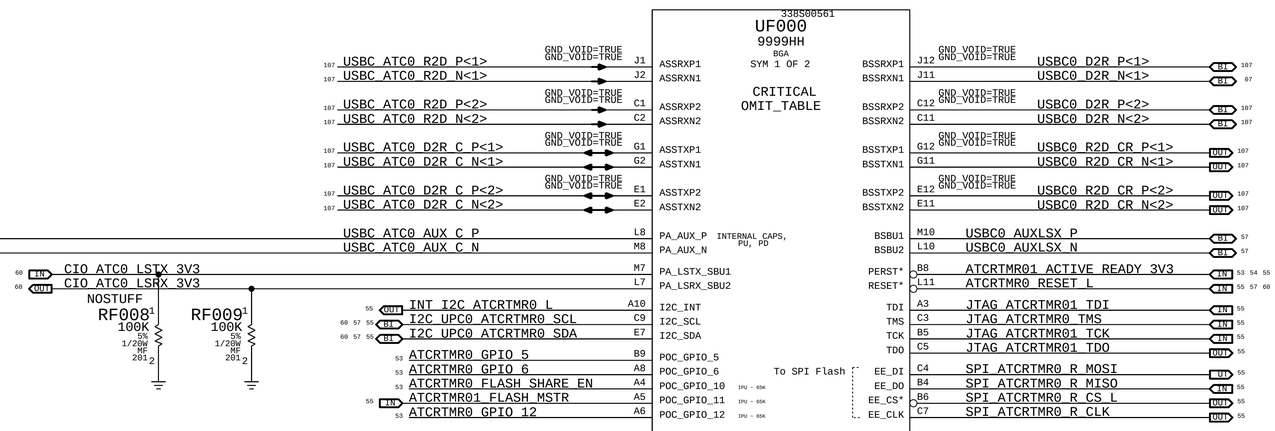
FAN

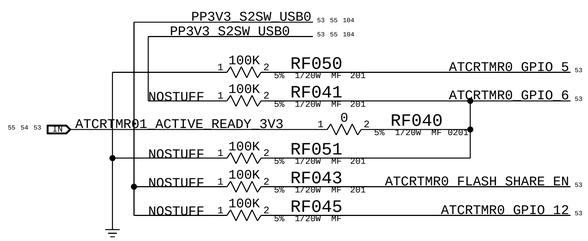
** OK2INTEGRATE **

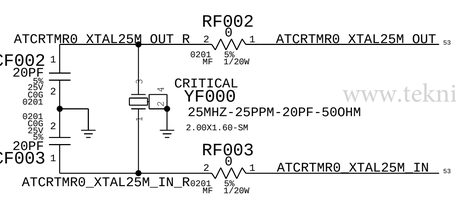
Caps and connector must be aliased to BBR signals.
Lanes 1 and 2 can be swapped, both pairs, both sides; all or nothing.
Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

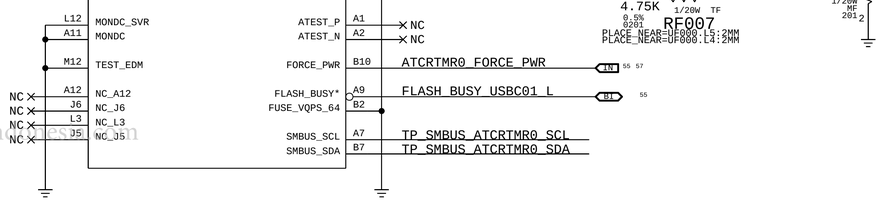
USBC HIGH-SPEED AC COUPLING

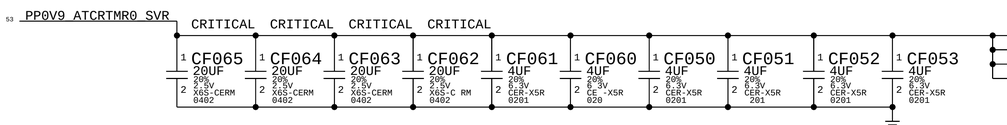


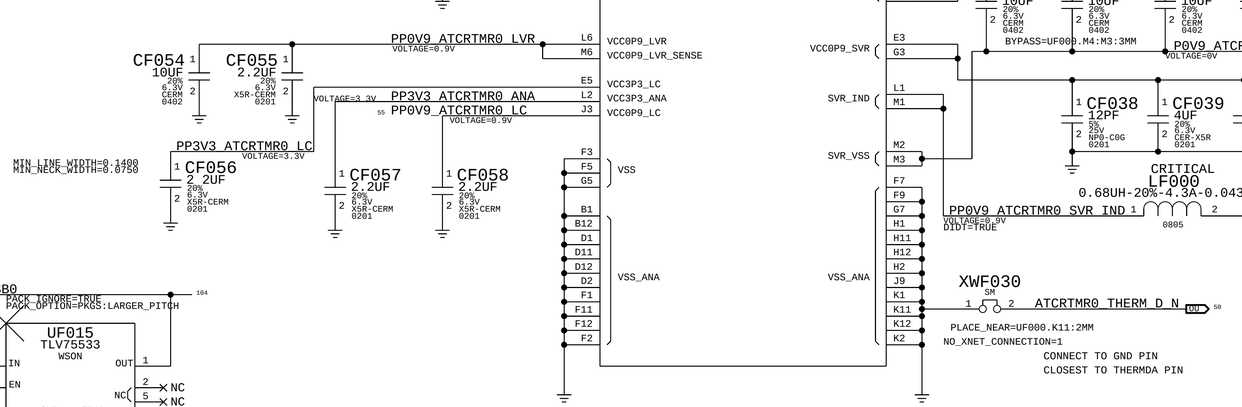




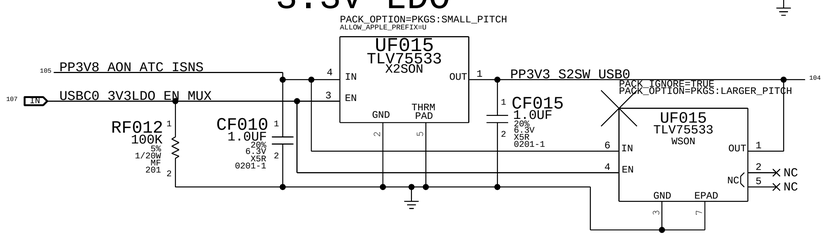








3.3V LDO



BOM_COST_GROUP=TBT

SYNC_MASTER=REF_USBC_ACE2 SYNC_DATE=02/14/2020

PAGE TITLE

USB-C: High Speed ATC0

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** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
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USBC HIGH-SPEED AC COUPLING

USBC_ATC1_R2D_C_P<1>	CF120 0.22UF	USBC_ATC1_R2D_P<1>	GND_VOID=TRUE; 20% X5R 6.3V 0201
USBC_ATC1_R2D_C_N<1>	CF121 0.22UF	USBC_ATC1_R2D_N<1>	GND_VOID=TRUE; 20% X5R 6.3V 0201
USBC_ATC1_R2D_C_P<2>	CF124 0.22UF	USBC_ATC1_R2D_P<2>	GND_VOID=TRUE; 20% X5R 6.3V 0201
USBC_ATC1_R2D_C_N<2>	CF125 0.22UF	USBC_ATC1_R2D_N<2>	GND_VOID=TRUE; 20% X5R 6.3V 0201
USBC_ATC1_D2R_P<1>	CF122 0.22UF	USBC_ATC1_D2R_C_P<1>	GND_VOID=TRUE; 20% X5R 6.3V 0201
USBC_ATC1_D2R_N<1>	CF123 0.22UF	USBC_ATC1_D2R_C_N<1>	GND_VOID=TRUE; 20% X5R 6.3V 0201
USBC_ATC1_D2R_P<2>	CF126 0.22UF	USBC_ATC1_D2R_C_P<2>	GND_VOID=TRUE; 20% X5R 6.3V 0201
USBC_ATC1_D2R_N<2>	CF127 0.22UF	USBC_ATC1_D2R_C_N<2>	GND_VOID=TRUE; 20% X5R 6.3V 0201
USBC_ATC1_AUX_P	CF128 0.1UF	USBC_ATC1_AUX_C_P	10% CERM-X5R 6.3V 0201
USBC_ATC1_AUX_N	CF129 0.1UF	USBC_ATC1_AUX_C_N	10% CERM-X5R 6.3V 0201

RF128[1] 33K 5% 1/20W MF 201
RF129[1] 33K 5% 1/20W MF 201

UF100 9999HH BGA SYM 1 OF 2

338S00561

CRITICAL OMIT_TABLE

Pin	Signal	Pin	Signal
J1	ASSRXP1	J12	BSSRXP1
J2	ASSRXN1	J11	BSSRXN1
C1	ASSRXP2	C12	BSSRXP2
C2	ASSRXN2	C11	BSSRXN2
G1	ASSTXP1	G12	BSSTXP1
G2	ASSTXN1	G11	BSSTXN1
E1	ASSTXP2	E12	BSSTXP2
E2	ASSTXN2	E11	BSSTXN2
L	PA_AUX_P (INTERNAL CAPS, PU, PD)	M10	BSBU1
M8	PA_AUX_N	L10	BSBU2
M7	PA_LSTX_SBU1	B8	PERST*
L7	PA_LSRX_SBU2	L11	RESET*
A10	I2C_INT	A3	TDI
C9	I2C_SCL	C3	TMS
E7	I2C_SDA	B5	TCK
B9	POC_GPIO_5	C5	TDO
A8	POC_GPIO_6	C4	EE_DI
A4	POC_GPIO_10 (IPU - 65K)	B4	EE_DO
A5	POC_GPIO_11 (IPU - 65K)	B6	EE_CS*
A6	POC_GPIO_12 (IPU - 65K)	C7	EE_CLK
M11	THERMDA	B11	TEST_EN
		B3	TEST_PWR_GOOD
L9	XTAL_25_IN	L4	RBIAS
M9	XTAL_25_OUT	L5	RSENSE
L12	MONDC_SVR	A1	ATEST_P
A11	MONDC	A2	ATEST_N
M12	TEST_EDM	B10	FORCE_PWR
A12	NC_A12	A9	FLASH_BUSY*
J6	NC_J6	B2	FUSE_VQPS_64
L3	NC_L3	A7	SMBUS_SCL
J5	NC_J5	B7	SMBUS_SDA

To SPI Flash

INT_I2C_ATCRTMR1_L	
I2C_UPC1_ATCRTMR1_SCL	
I2C_UPC1_ATCRTMR1_SDA	
ATCRTMR1_GPIO_5	
ATCRTMR1_GPIO	
ATCRTMR1_FLASH_SHARE_EN	
ATCRTMR01_FLASH_SLV_L	
ATCRTMR1_GPIO_12	
ATCRTMR1_THERM_D_P	
ATCRTMR1_XTAL25M_IN	
ATCRTMR1_XTAL25M_OUT	
USBC1_D2R_P<1>	
USBC1_D2R_N<1>	
USBC1_D2R_P<2>	
USBC1_D2R_N<2>	
USBC1_R2D_CR_P<1>	
USBC1_R2D_CR_N<1>	
USBC1_R2D_CR_P<2>	
USBC1_R2D_CR_N<2>	
USBC1_AUXLSX_P	
USBC1_AUXLSX_N	
ATCRTMR01_ACTIVE_READY_3V3	
JTAG_ATCRTMR01_TDI	
JTAG_ATCRTMR1_TMS	
JTAG_ATCRTMR01_TCK	
JTAG_ATCRTMR01_TDO	
SPI_ATCRTMR1_R_MOSI	
SPI_ATCRTMR1_R_MISO	
SPI_ATCRTMR1_R_CS_L	
SPI_ATCRTMR1_R_CLK	
ATCRTMR1_TEST_PWR_GOOD	
ATCRTMR1_RBIAS	
ATCRTMR1_RSENSE	
NC	
NC	
ATCRTMR1_FORCE_PWR	
FLASH_BUSY_USBC01_L	
TP_SMBUS_ATCRTMR1_SCL	
TP_SMBUS_ATCRTMR1_SDA	

CIO_ATC1_LSTX_3V3
CIO_ATC1_LSRX_3V3
NOSTUFF
RF108[1] 100K 5% 1/20W MF 201
RF109[1] 100K 5% 1/20W MF 201
RF106[1] 100 5% 1/20W MF 201
4.75K 0.5% 0201 RF107 1/20W TF
PLACE_NEAR=UF100.L5:2MM
PLACE_NEAR=UF100.L4:2MM

PP3V3_S2SW_USB1
PP3V3_S2SW_USB1

100K	RF150	ATCRTMR1_GPIO_5
NOSTUFF 100K	RF141	ATCRTMR1_GPIO_6
ATCRTMR01_ACTIVE_READY_3V3	RF140 0	
NOSTUFF 100K	RF151	
NOSTUFF 100K	RF143	ATCRTMR1_FLASH_SHARE_EN
NOSTUFF 100K	RF145	ATCRTMR1_GPIO_12

ATCRTMR1_XTAL25M_OUT_R — RF102 0 — ATCRTMR1_XTAL25M_OUT
CF102 20PF 25V C0G 0201
CRITICAL YF100 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
CF103 20PF 25V C0G 0201
ATCRTMR1_XTAL25M_IN_R — RF103 0 — ATCRTMR1_XTAL25M_IN

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UF100 9999HH BGA SYM 2 OF 2

338S00561

CRITICAL OMIT_TABLE

Pin	Signal	Pin	Signal
F6	VCC0P9_SVR_ANA	E6	VCC3P3_SX
G6		J7	VCC3P3A
E9	VCC0P9_SVR_PB_ANA	M4	VCC3P3_SVR
G9		M5	
L6	VCC0P9_LVR	E3	VCC0P9_SVR
M6	VCC0P9_LVR_SENSE	G3	
E5	VCC3P3_LC	L1	SVR_IND
L2	VCC3P3_ANA	M1	
J3	VCC0P9_LC	M2	SVR_VSS
F3	VS	M3	
F5		F7	VSS_ANA
G5		F9	
B1	VSS_ANA	G7	
B12		H1	
D1		H11	
D11		H12	
D12		H2	
D2		J9	
F1		K1	
F11		K11	
F12		K12	
F2		K2	

PP0V9_ATCRTMR1_SVR — CRITICAL CF165 20UF 6.3V X6S-CERM 0402; CF164 20UF; CF163 20UF; CF162 20UF; CF161 4UF 6.3V CER-X5R 0201; CF160 4UF; CF150 4UF; CF151 4UF; CF152 4UF; CF153 4UF

PP0V9_ATCRTMR1_LVR VOLTAGE=0.9V — CF154 10UF 6.3V CERM 0402; CF155 2.2UF 6.3V X5R-CERM 0201
PP3V3_ATCRTMR1_ANA VOLTAGE=3.3V
PP0V9_ATCRTMR1_LC VOLTAGE=0.9V
PP3V3_ATCRTMR1_LC VOLTAGE=3.3V — CF156 2.2UF 6.3V X5R-CERM 0201
CF157 2.2UF 6.3V X5R-CERM 0201; CF158 2.2UF 6.3V X5R-CERM 0201
MIN_LINE_WIDTH=0.1400 MIN_NECK_WIDTH=0.0750

FROM USB-C PORT CONTROLLER (UPC) PP3V3_S2SW_USB1
CF136 2.2UF 6.3V X5R-CERM 0201; CF137 2.2UF 6.3V X5R-CERM 0201; NOSTUFF CF142 47UF 6.3V CER-X5R 0603
VOLTAGE=3.3V PP3V3_ATCRTMR1_VCCA — CF143 12PF 25V NP0-C0G 0201; CF130 2.2UF 6.3V X5R-CERM 0201; CF131 10UF 6.3V CERM 0402
RF100 0 5% 1/16W MF-LF 402
RF101 0 5% 1/16W MF-LF 402
XWF101 SM NO_XNET_CONNECTION=1 — PP3V3_S2SW_USB1
PP3V3_ATCRTMR1_SVR — CF132 10UF; CF133 10UF; CF134 10UF; CF135 10UF 6.3V CERM 0402
BYPASS=UF100.M4:M3:3MM
P0V9_ATCRTMR1_SVR_PGND VOLTAGE=0V
XWF100 SM PLACE_NEAR=CF132.2:2MM NO_XNET_CONNECTION=1 — PP0V9_ATCRTMR1_SVR VOLTAGE=0.9V
CF138 12PF 25V NP0-C0G 0201; CF139 4UF 6.3V CER-X5R 0201; CF141 4UF 6.3V CER-X5R 0201
CRITICAL LF100 0.68UH-20%-4.3A-0.043OHM 0805
PP0V9_ATCRTMR1_SVR_IND VOLTAGE=0.9V DIDT=TRUE
CF140 47UF 6.3V CER-X5R 0603

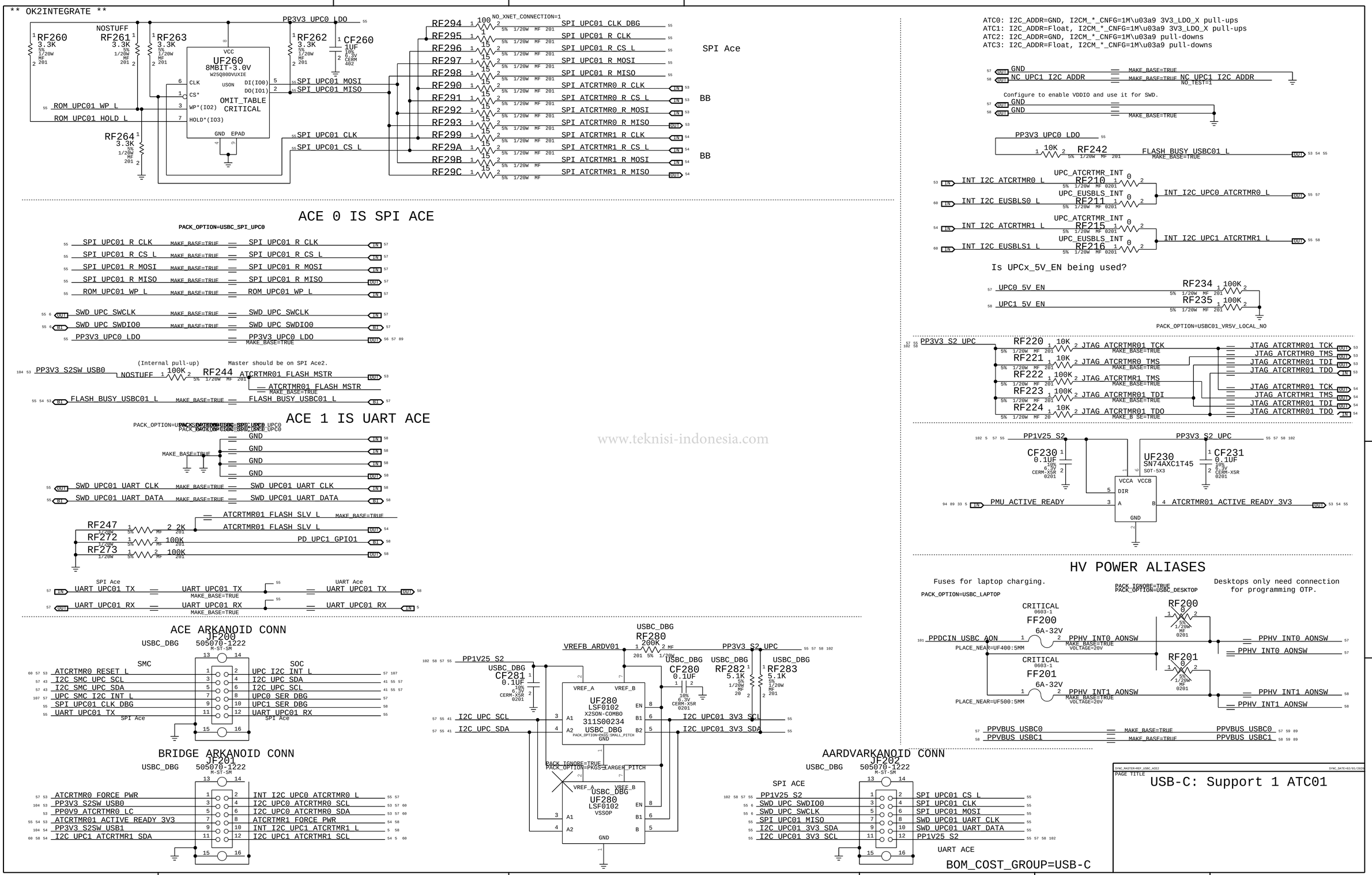
3.3V LDO

PACK_OPTION=PKGS:SMALL_PITCH ALLOW_APPLE_PREFIX=U
UF115 TLV75533 X2SON — IN, EN, OUT, GND, THRM PAD
PP3V8_AON_ATC_ISNS
USBC1_3V3LDO_EN
RF112 100K 5% 1/20W MF 201
CF110 1.0UF 20% 6.3V X5R 0201-1
CF115 1.0UF 20% 6.3V X5R 0201-1
PACK_IGNORE=TRUE PACK_OPTION=PKGS:LARGER_PITCH
UF115 TLV75533 WSON — IN, EN, OUT, GND, EPAD

XWF130 SM — ATCRTMR1_THERM_D_N
PLACE_NEAR=UF100.K11:2MM
NO_XNET_CONNECTION=1
CONNECT TO GND PIN
CLOSEST TO THERMDA PIN

BOM_COST_GROUP=TBT

SYNC_MASTER=REF_USBC_ACE2 SYNC_DATE=02/14/2020
PAGE TITLE
USB-C: High Speed ATC1



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** OK2INTEGRATE **

Ace 0 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC0

ATC0 / UPC0 / RTMR0

89 18 6 IN	UART_DEBUGPRT_R2D	MAKE_BASE=TRUE	UART_DEBUGPRT_R2D	IN 57 96
89 18 6 OUT	UART_DEBUGPRT_D2R	MAKE_BASE=TRUE	UART_DEBUGPRT_D2R	IN 57 96
89 18 9 BI	SWD_SOC_SWCLK	MAKE_BASE RUE	SWD_SOC_SWCLK	OUT 57 96
89 18 9 BI	SWD_SOC_SWDIO	MAKE_BASE=TRUE	SWD_SOC_SWDIO	OUT 57 96
89 9 IN	UART_SMC_DEBUGPRT_R2D	MAKE_BASE=TRUE	UART_SMC_DEBUGPRT_R2D	OUT 57 96
89 9 OUT	UART_SMC_DEBUGPRT_D2R	MAKE_BASE=TRUE	UART_SMC_DEBUGPRT_D2R	IN 57 96
96 89 BI	USB_DBG_LS_P	MAKE_BASE=TRUE	USB_DBG_LS_P	BI 57
96 89 BI	USB_DBG_LS_N	MAKE_BASE=TRUE	USB_DBG_LS_N	BI 57
	PP1V8_S2		PP1V8_S2	BI 57 60 101
	PP1V8_S2		PP1V8_S2	BI 60 101
107 OUT	UPC0_GPIO7		UPC0_GPIO7	IN 57 96 107
94 89 19 5 IN	SOC_DFU_STATUS	MAKE_BASE=TRUE	SOC_DFU_STATUS	OUT 57
90 89 33 5 OUT	SOC_FORCE_DFU	MAKE_BASE=TRUE	SOC_FORCE_DFU	IN 57

Main Debug Port

Ace 1 is non-debug Port?

PACK_OPTION=USBC_DEBUG_UPC0

ATC1 / UPC1 / RTMR1

	PP1V8_S2		PP1V8_S2	BI 58 60 101
	PP1V8_S2_USBLS1_ISNS		PP1V8_S2_USBLS1_ISNS	BI 60 105
RF320 1/20W 1 5% 2 MF 100K 201	PD_UPC1_DBG0_R	MAKE_BASE=TRUE	PD_UPC1_DBG0_R	BI 58
RF321 1/20W 1 5% 2 MF 100K 201	PD_UPC1_DBG1_R	MAKE_BASE=TRUE	PD_UPC1_DBG1_R	BI 58
RF322 1/20W 1 5% 2 MF 100K 201	PD_UPC1_DBG2_R	MAKE_BASE=TRUE	PD_UPC1_DBG2_R	BI 58
RF323 1/20W 1 5% 2 MF 100K 201	PD_UPC1_DBG3_R	MAKE_BASE=TRUE	PD_UPC1_DBG3_R	BI 58
RF324 1/20W 1 5% 2 MF 100K 201	PD_UPC1_DBG4_R	MAKE_BASE=TRUE	PD_UPC1_DBG4_R	BI 58
RF325 1/20W 1 5% 2 MF 100K 201	PD_UPC1_DBG5_R	MAKE_BASE=TRUE	PD_UPC1_DBG5_R	BI 58
RF328 1/20W 1 5% 2 MF 100K 201	PD_UPC1_USBP2_RP	MAKE_BASE=TRUE	PD_UPC1_USBP2_RP	BI 58
RF329 1/20W 1 5% 2 MF 100K 201	PD_UPC1_USBP2_RN	MAKE_BASE=TRUE	PD_UPC1_USBP2_RN	BI 58
RF373 1/20W 1 5% 2 MF 100K 201	PD_UPC1_GPIO7	MAKE_BASE=TRUE	PD_UPC1_GPIO7	OUT 58
RF374 1/20W 1 5% 2 MF 100K 201	PD_UPC1_GPIO9	MAKE_BASE=TRUE	PD_UPC1_GPIO9	OUT 58
RF375 1/20W 1 5% 2 M 100K 201	PD_UPC1_GPIO10	MAKE_BASE=TRUE	PD_UPC1_GPIO10	OUT 58

Ace2 GPIOs

CKPLUS_WAIVE=SINGLE_NODENET
on all nets above.

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Non-debug Port

Unused ports

RF316 1/20W 1 5% 2 MF 100K 201	PD_UPC0_DBG6_R	MAKE_BASE=TRUE	PD_UPC0_DBG6_R BI 57
RF317 1/20W 1 5% 2 MF 100K 201	PD_UPC0_DBG7_R	MAKE_BASE=TRUE	PD_UPC0_DBG7_R BI 57
RF31A 1/20W 1 5% 2 MF 100K 201	PD_UPC0_USBP3_RP	MAKE_BASE=TRUE	PD_UPC0_USBP3_RP BI 57
RF31B 1/20W 1 5% 2 MF 100K 201	PD_UPC0_USBP3_RN	MAKE_BASE=TRUE	PD_UPC0_USBP3_RN BI 57
RF326 1/20W 1 5% 2 MF 100K 201	PD_UPC1_DBG6_R	MAKE_BASE=TRUE	PD_UPC1_DBG6_R BI 58
RF327 1/20W 1 5% 2 MF 100K 201	PD_UPC1_DBG7_R	MAKE_BASE=TRUE	PD_UPC1_DBG7_R BI 58
RF32A 1/20W 1 5% 2 MF 100K 201	PD_UPC1_USBP3_RP	MAKE_BASE RUE	PD_UPC1_USBP3_RP B 58
RF32B 1/20W 1 5% 2 MF 100K 201	PD_UPC1_USBP3_RN	MAKE_BASE=TRUE	PD_UPC1_USBP3_RN BI 58

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP

57 OUT	PP3V3_UPC0_LDO	MAKE_BASE=TRUE	PP3V3_UPC0_LDO	IN 55 57 89
5 BI	USBC0_CC1	MAKE_BASE=TRUE	USBC0_CC1	BI 57 59 89
57 BI	USBC0_CC2	MAKE_BASE=TRUE	USBC0_CC2	BI 57 59 89
58 OUT	PP3V3_UPC1_LDO	MAKE_BASE=TRUE	PP3V3_UPC1_LDO	IN 58
58 BI	USBC1_CC1	MAKE_BASE=TRUE	USBC1_CC1	BI 58 59 89
58 BI	USBC1_CC2	MAKE_BASE=TRUE	USBC1_CC2	BI 58 59 89

BOM_COST_GROUP=USB-C

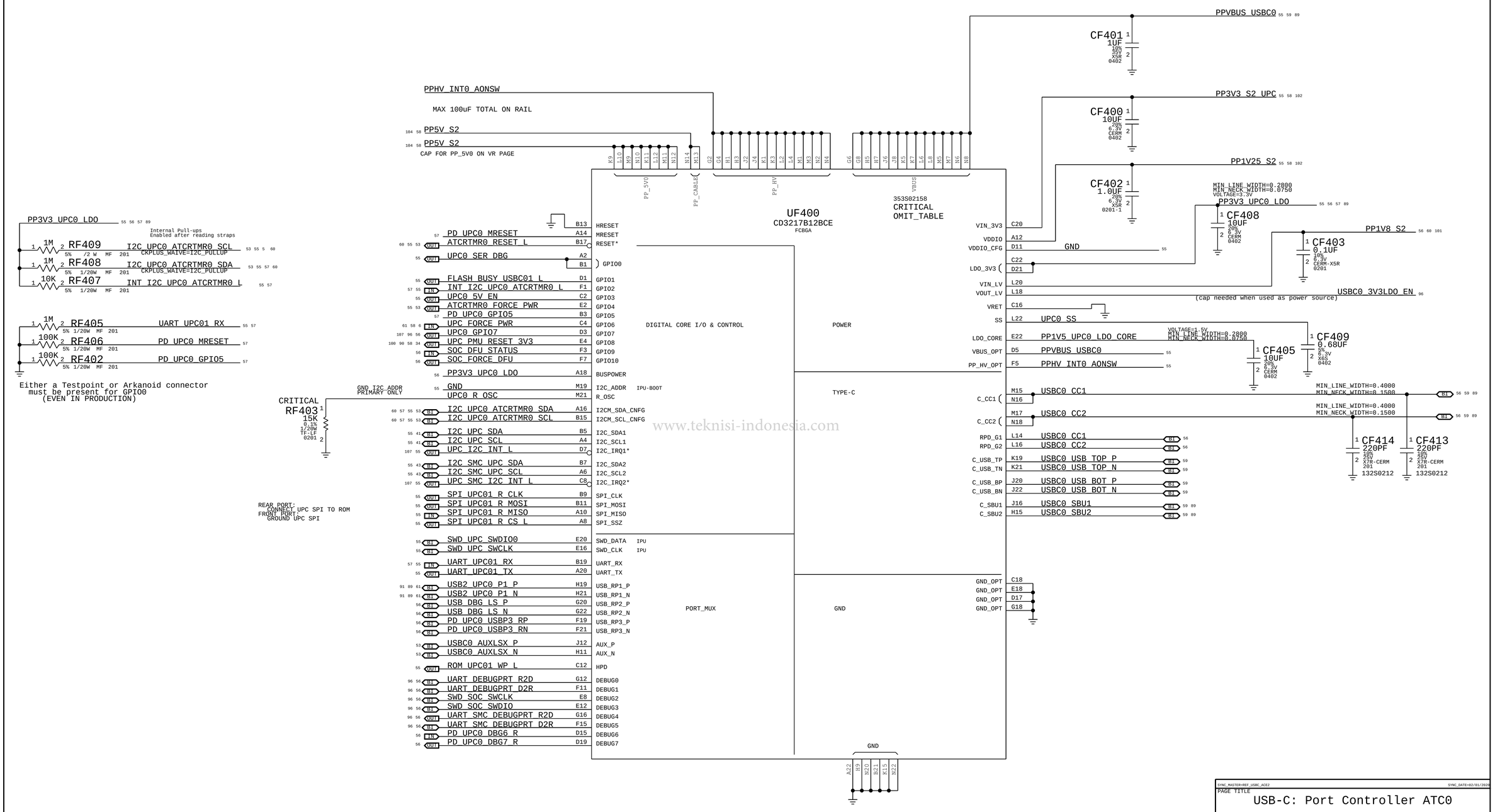
SYNC_MASTER=REF_USBC_ACE2 SYNC_DATE=02/01/2020

PAGE TITLE

USB-C: Support 2 ATC01

A

2 1



BOM_COST_GROUP=USB-C

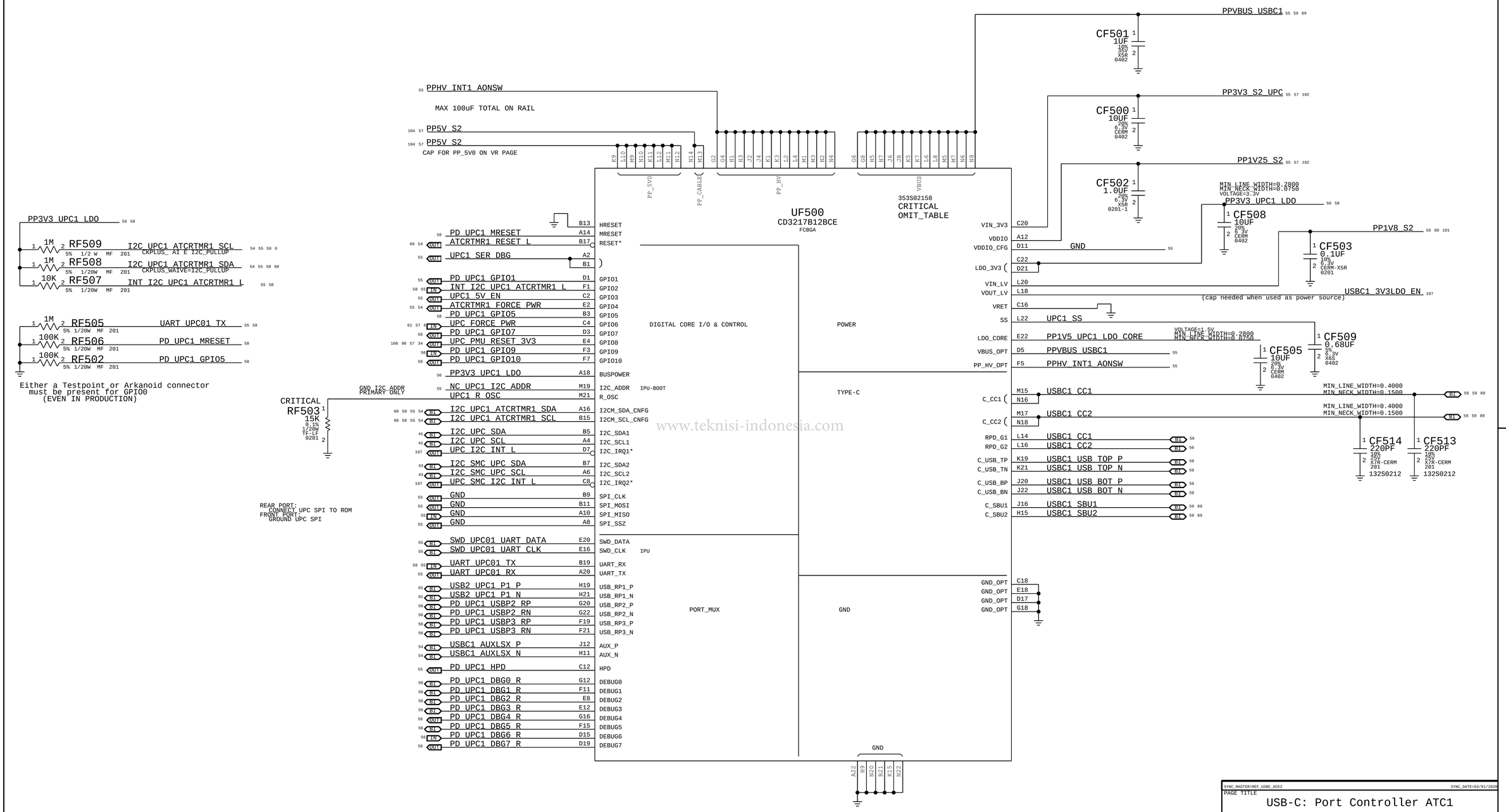
SYNC_MASTER=REF_USBC_ACE2 SYNC_DATE=02/01/2020

PAGE TITLE

USB-C: Port Controller ATC0

A

** OK2INTEGRATE **



SYNC_MASTER=REF_USBC_ACE2 SYNC_DATE=02/01/2020

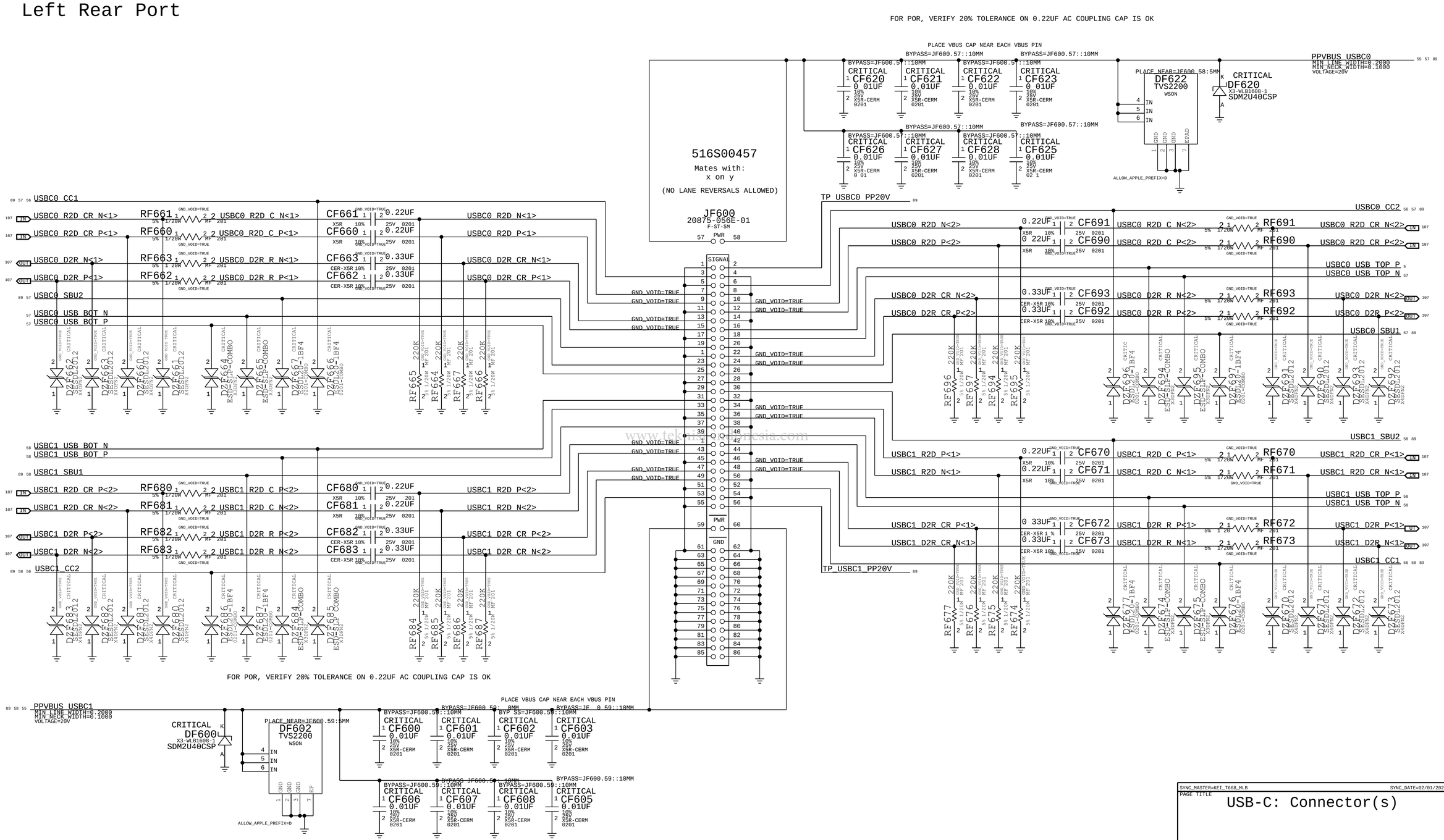
PAGE TITLE

USB-C: Port Controller ATC1

BOM COST GROUP=USB-C

---- Reference only ----

Left Rear Port



Left Front Port

SYNC_MASTER=KEI_T668_MLB	SYNC_DATE=02/01/2020
PAGE TITLE	USB-C: Connector(s)

BOM_COST_GROUP=USB-C

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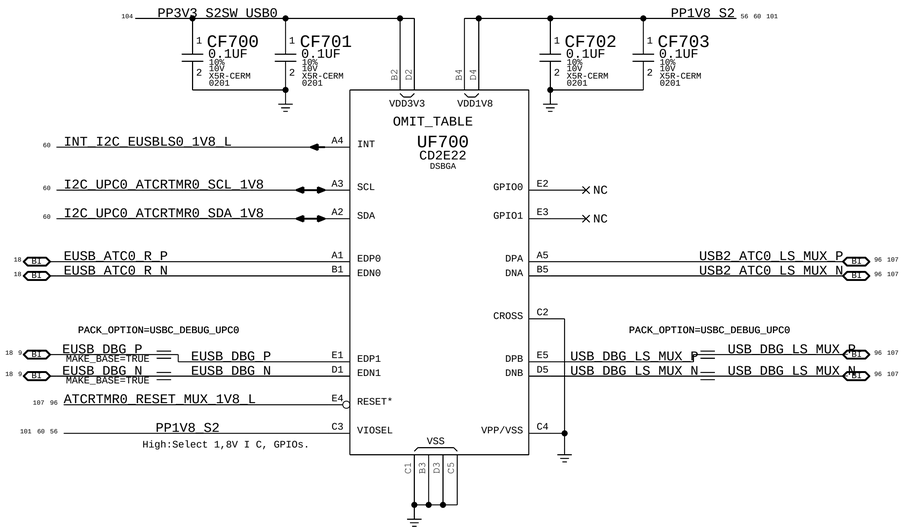
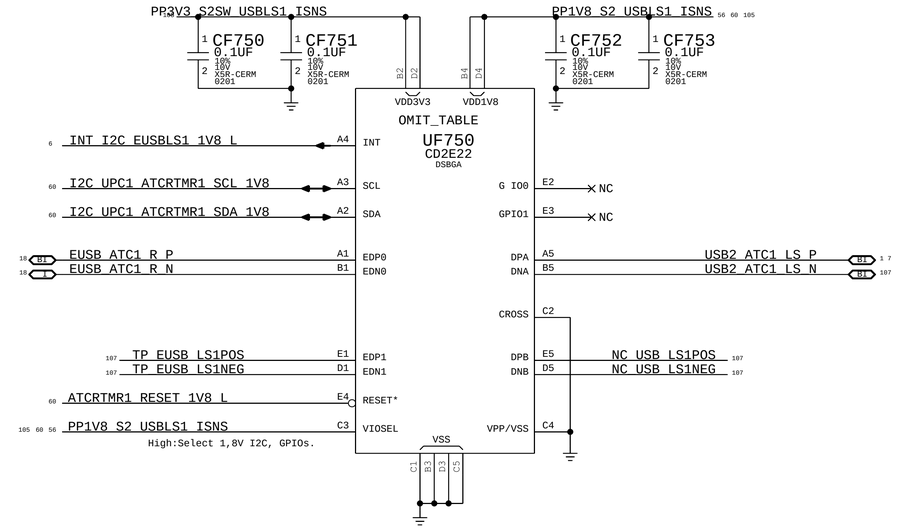
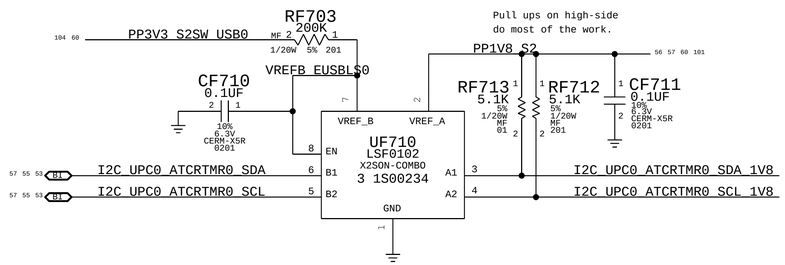
** OK2INTEGRATE **

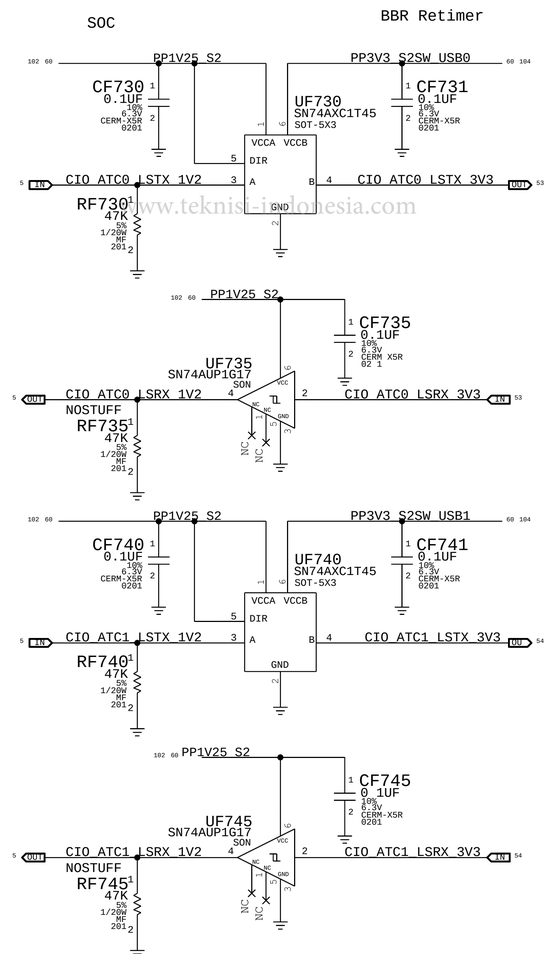




PARROT 0 I2C/RESET LEVEL SHIFTERS



TBT LS RX/TX LEVEL SHIFTERS



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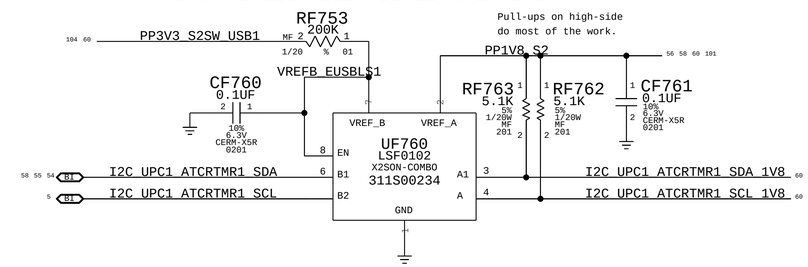
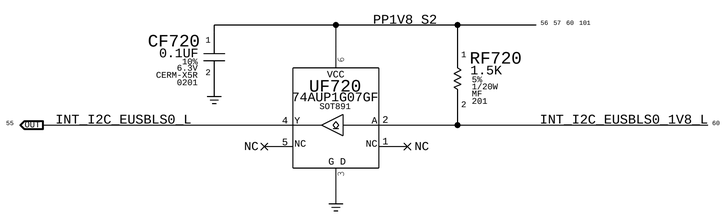
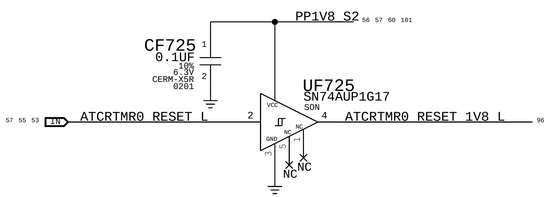
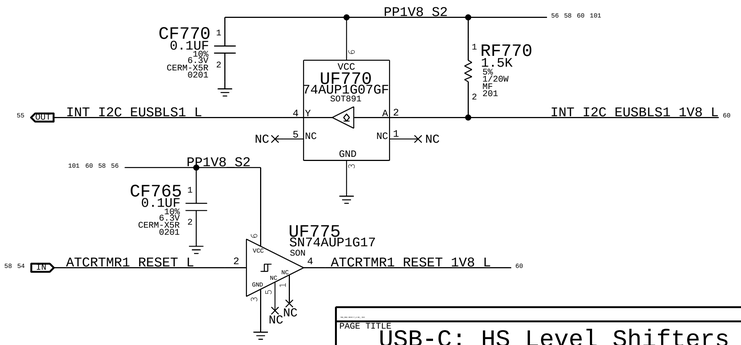
PARROT 1 I2C/RESET LEVEL SHIFTERS





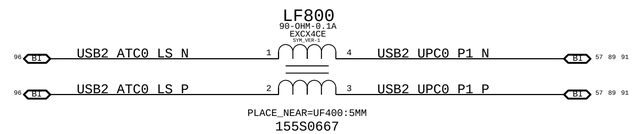


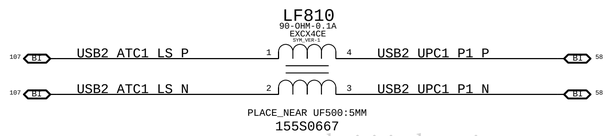


PAGE TITLE

USB-C: HS Level Shifters

BOM_COST_GROUP=USB-C





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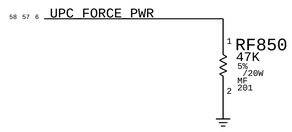
NOTE: CHOKE PINOUT IS DIFFERENT BETWEEN LANE 0 AND LANE 1 FOR EASE OF ROUTING

<RDAR://59047957>



PAGE TITLE

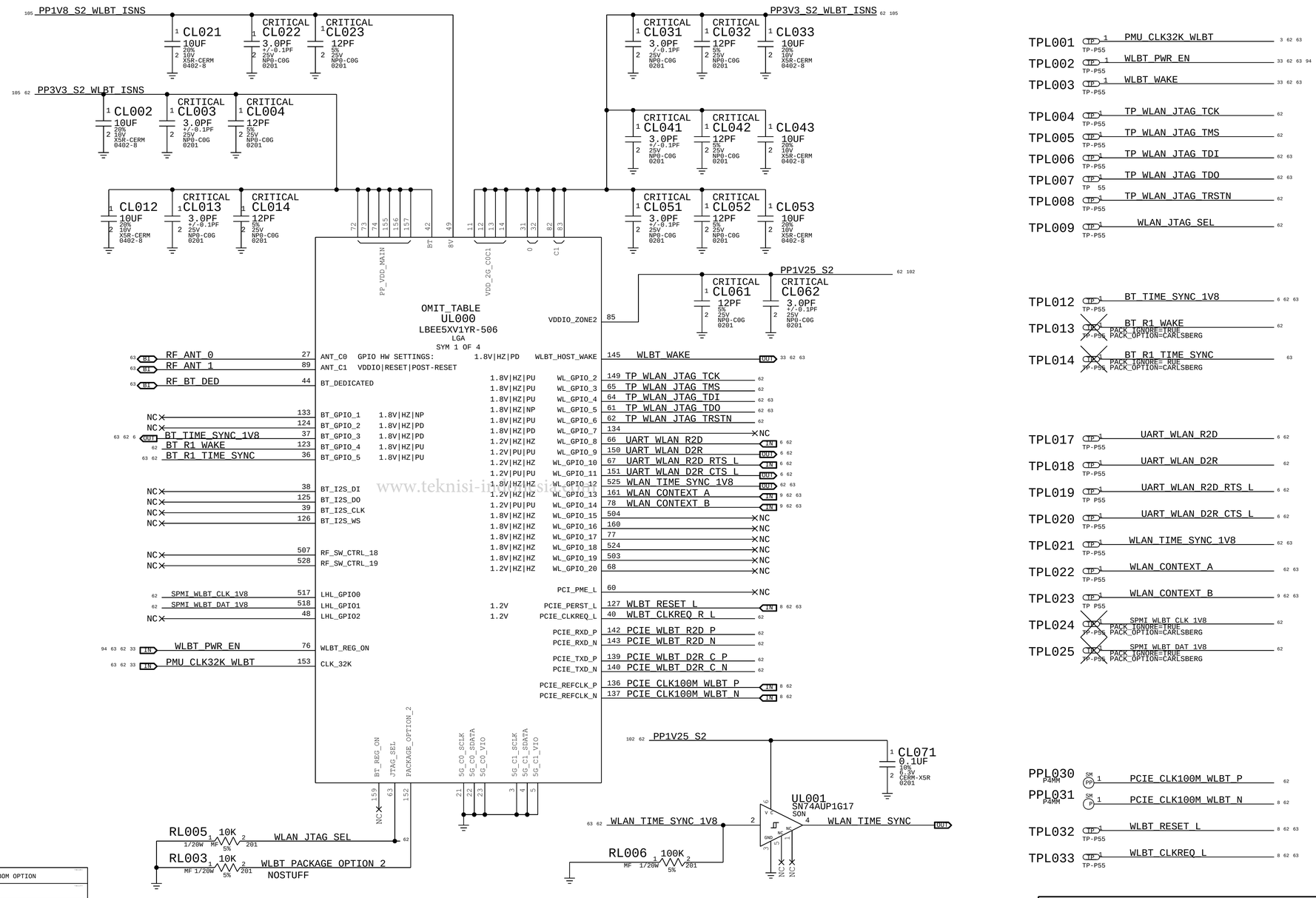
USB-C: SUPPORT

BOM_COST_GROUP=USB-C

*** OK2INTEGRATE ***

RASPUTIN WIFI/BT MODULE

FOR HOSTINTERFACE TABLES REFER TO
RDAR://PROBLEM/53187294



RASPUTIN BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00763	1	MODULE, WLAN BT, RASPUTIN, ES6.11, M, LGA549	UL000	CRITICAL	

PAGE TITLE: WIFI/BT: MODULE

DRAWING NUMBER | SIZE

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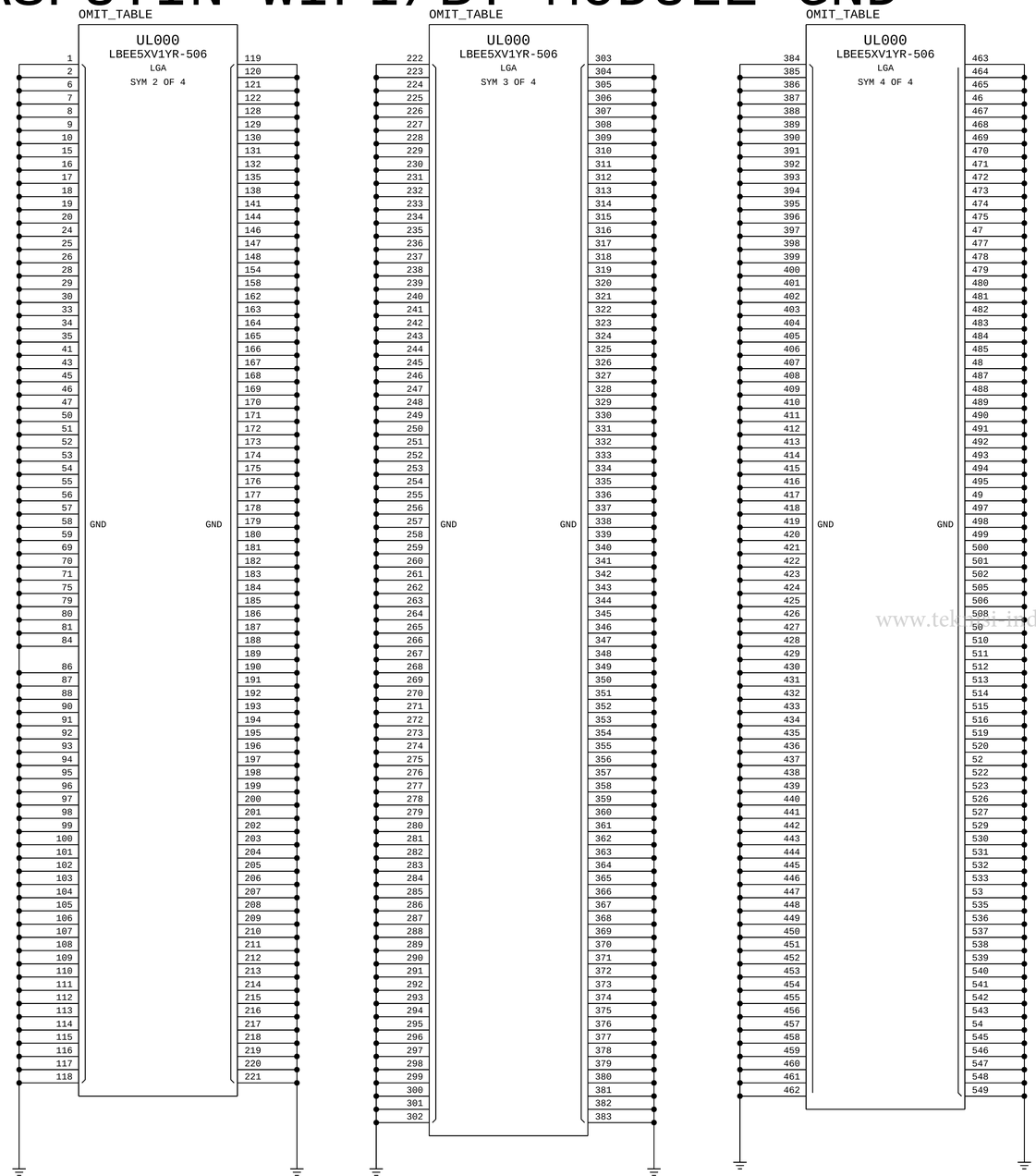
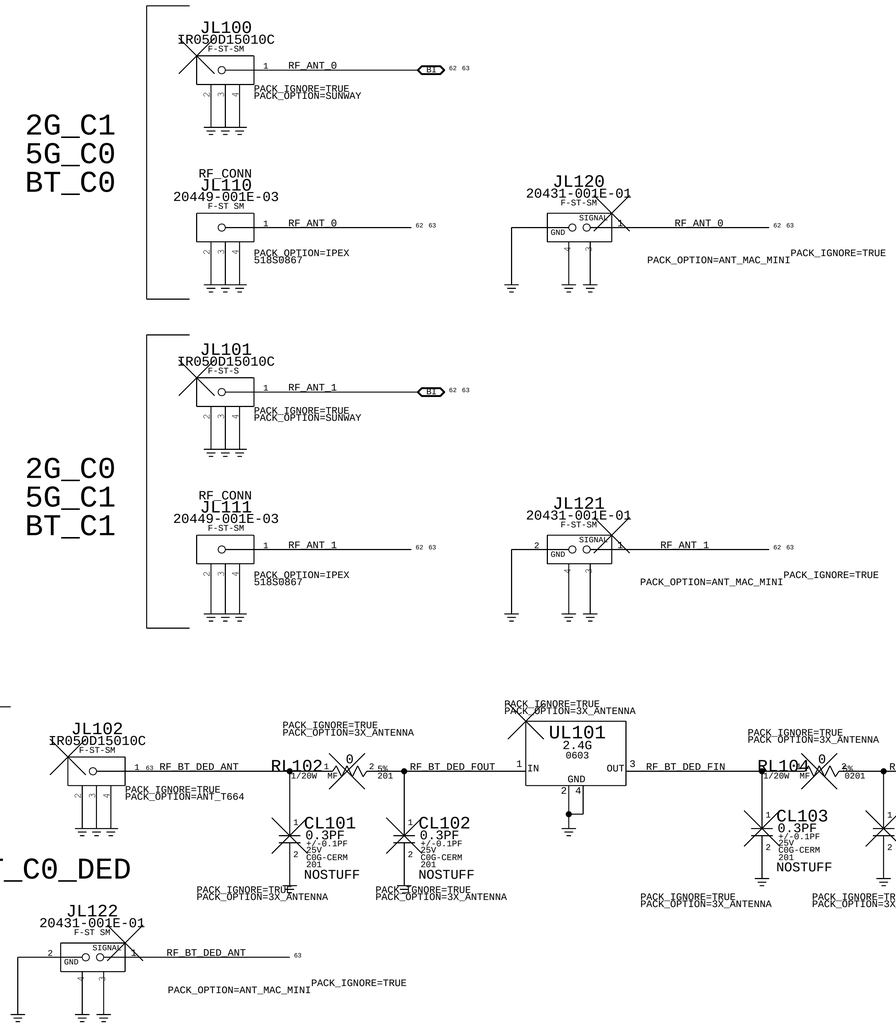
*** OK2INTEGRATE ***

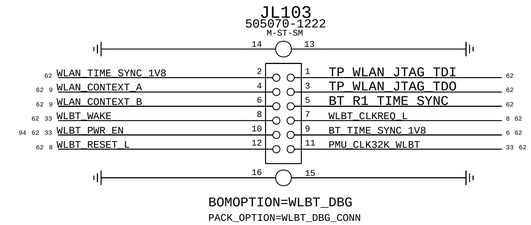
RASPUTIN WIFI/BT MODULE GND



ANTENNA CONNECTORS



WLBT DEBUG CONNECTOR



BOMOPTION=WLBT_DBG
PACK_OPTION=WLBT_DBG_CONN

BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT: ANTENNA and GND

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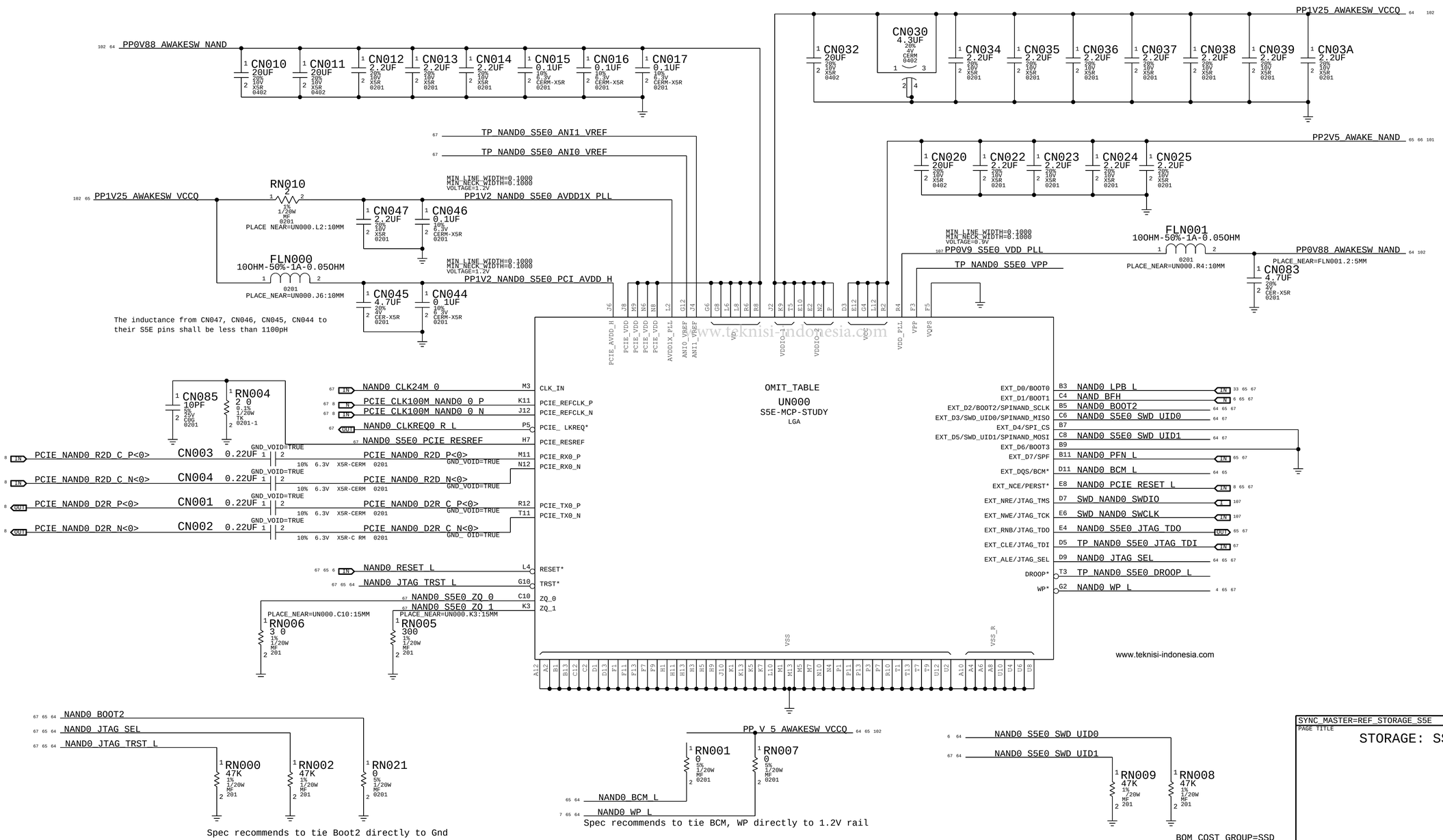
*** OK2INTEGRATE ***

NAND0 S5E0



SYNC_MASTER=REF_STORAGE_S5E SYNC_DATE=04/27/2020

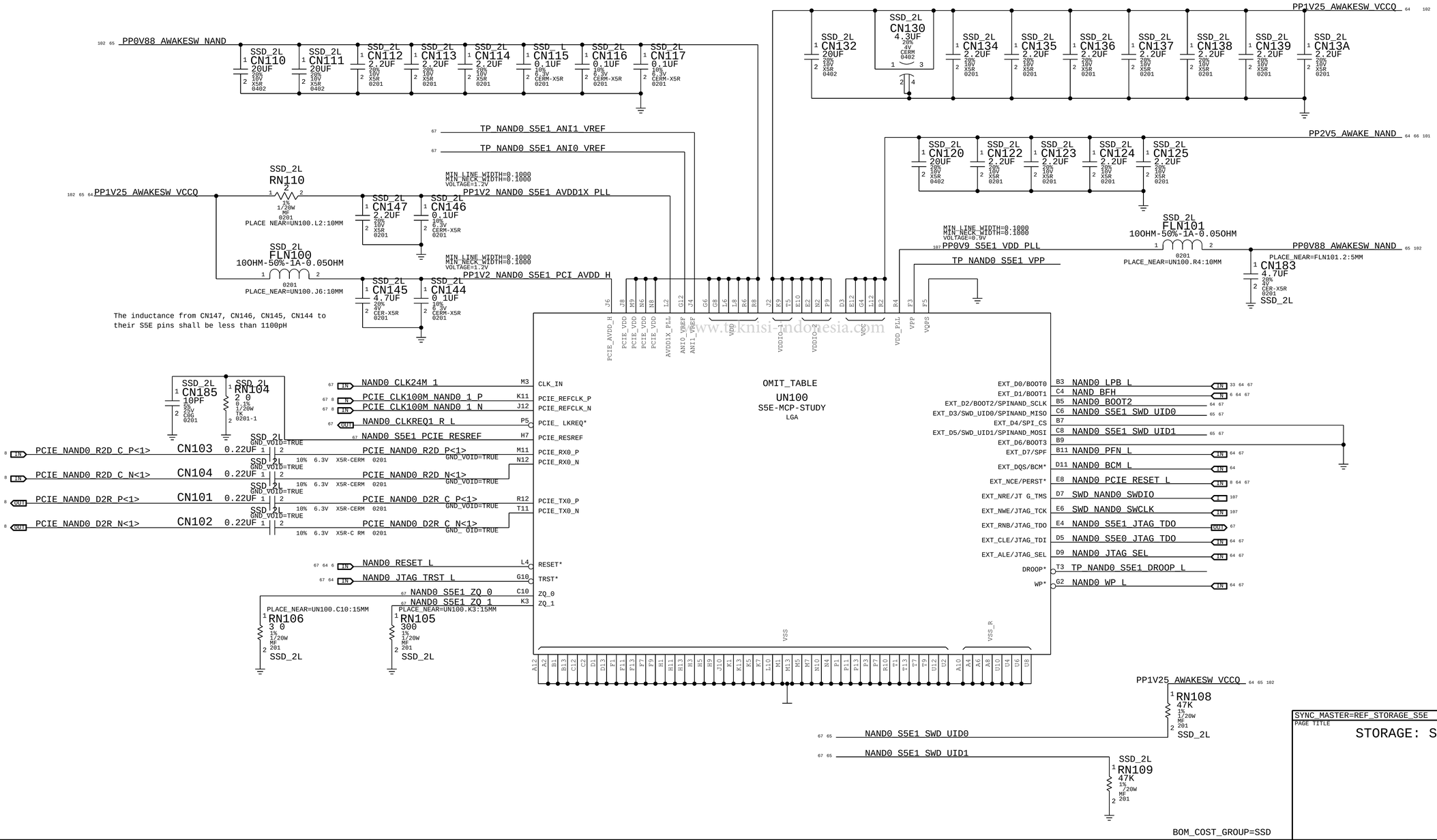
PAGE TITLE

STORAGE: SSD0 S5E <0>

5 3 2 1

*** OK2INTEGRATE ***

NAND0 S5E1



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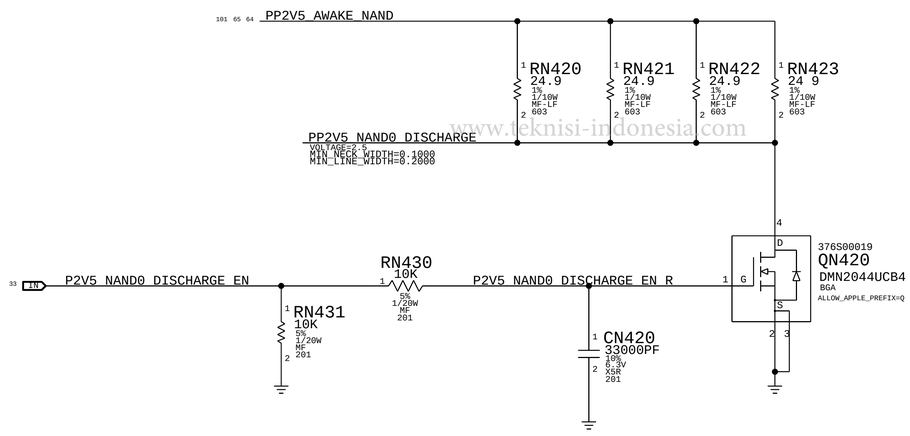
3 2 1

OK2INTEGRATE

THIS EXTERNAL NAND VCC DISCHARGE CIRCUITRY IS FOR SYSTEM THAT DOES NOT USE OCARINA



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SYNC_MASTER=REF STORAGE_N N OCARINA_SUPPORT SYNC_DATE=02/25/2020

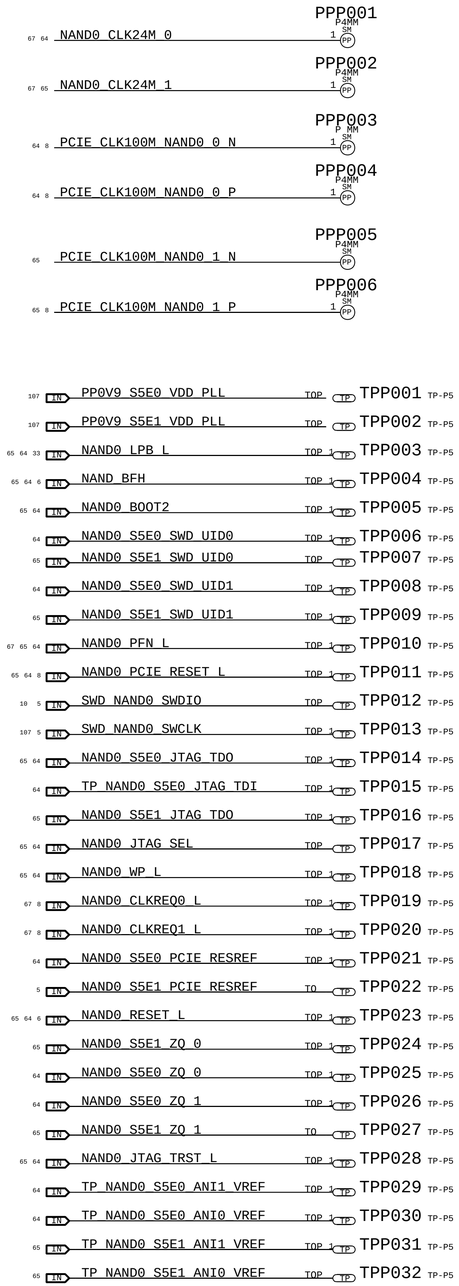
PAGE TITLE

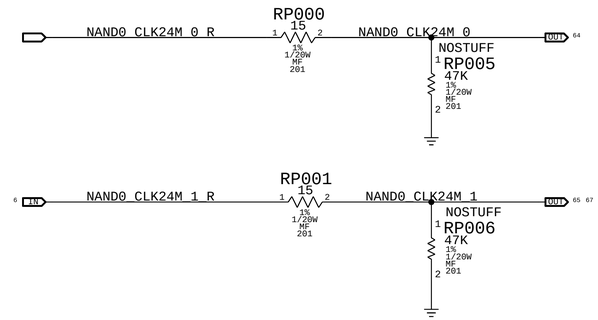
STORAGE: NON OCARINA SUPPORT

A

2 1

SSD 24M CLOCK TERMINATIONS





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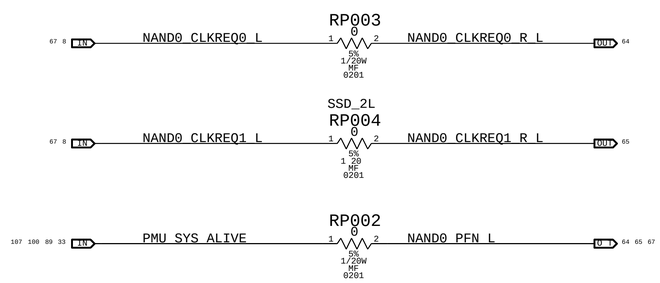


BOM_COST_GROUP=SSD

PAGE TITLE

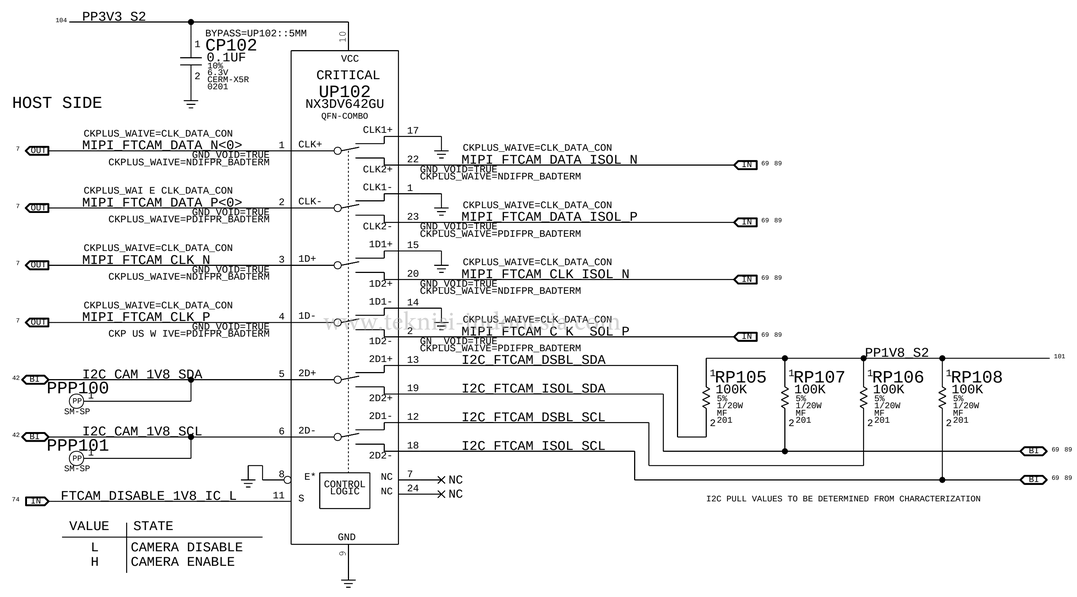
STORAGE: SSD SUPPORT

A

2 1

*** OK2INTEGRATE ***

CAMERA SECURE DISABLE



VALUE	STATE
L	CAMERA DISABLE
H	CAMERA ENABLE

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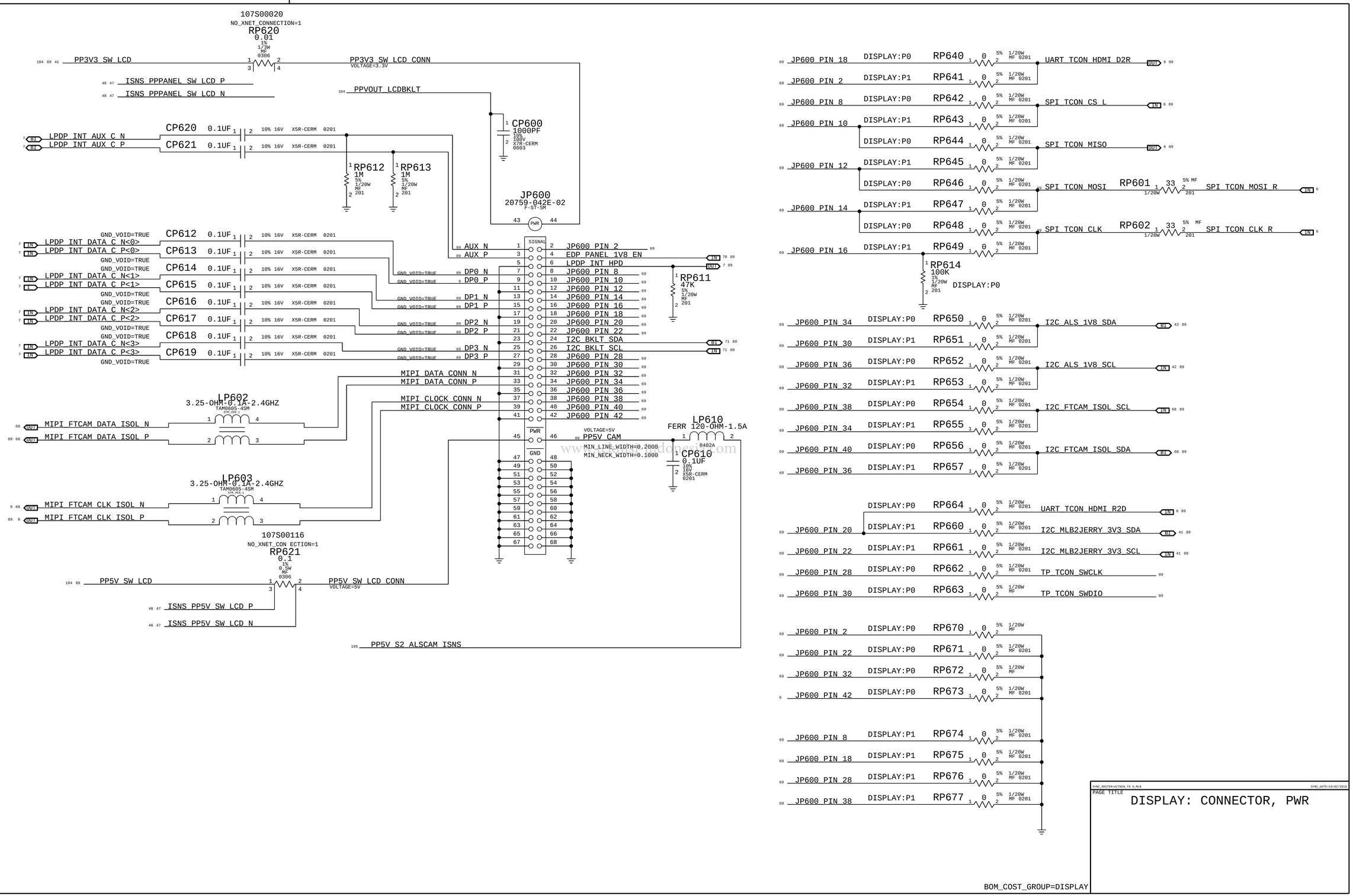
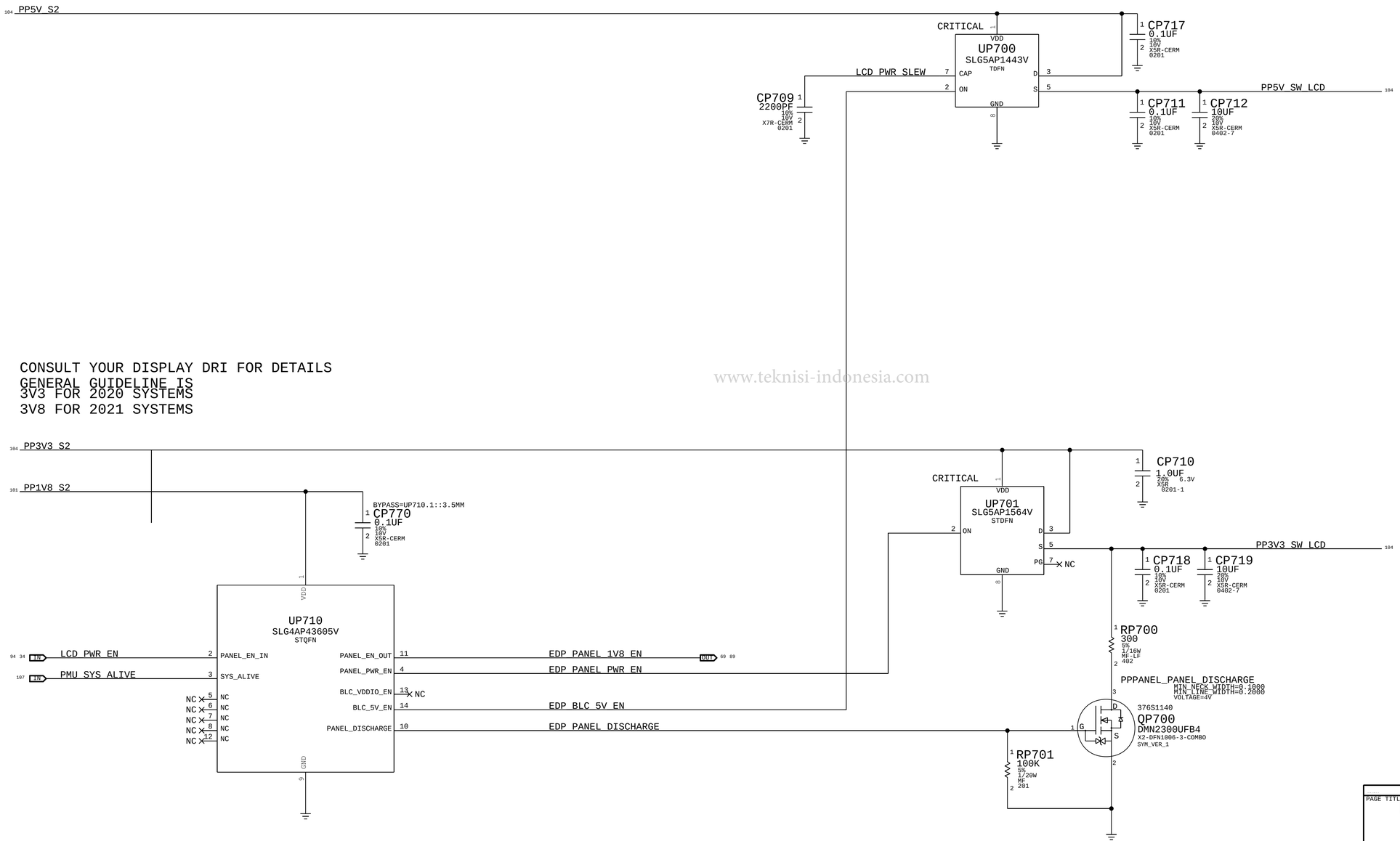
PAGE TITLE

SECDIS: MIPI MUX

BOM_COST_GROUP=CAMERA


107S00020
NO_XNET_CONNECTION=1
RP620
0.01
1%
1/3W
MF
0306
PP3V3_SW_LCD
PP3V3_SW_LCD_CONN
VOLTAGE=3.3V
ISNS_PPPANEL_SW_LCD_P
ISNS_PPPANEL_SW_LCD_N
PPVOUT_LCDBKLT
CP600
1000PF
10%
16V
X7R-CERM
0603
CP620 0.1UF 10% 16V X5R-CERM 0201
CP621 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_AUX_C_N
LPDP_INT_AUX_C_P
RP612
1M
5%
1/20W
MF
201
RP613
1M
5%
1/20W
MF
201
JP600
20759-042E-02
F-ST-SM
PWR
SIGNAL
GND
CP612 0.1UF
CP613 0.1UF
CP614 0.1UF
CP615 0.1UF
CP616 0.1UF
CP617 0.1UF
CP618 0.1UF
CP619 0.1UF
GND_VOID=TRUE
LPDP_INT_DATA_C_N<0>
LPDP_INT_DATA_C_P<0>
LPDP_INT_DATA_C_N<1>
LPDP_INT_DATA_C_P<1>
LPDP_INT_DATA_C_N<2>
LPDP_INT_DATA_C_P<2>
LPDP_INT_DATA_C_N<3>
LPDP_INT_DATA_C_P<3>
AUX_N
AUX_P
DP0_N
DP0_P
DP1_N
DP1_P
DP2_N
DP2_P
DP3_N
DP3_P
JP600_PIN_2
EDP_PANEL_1V8_EN
LPDP_INT_HPD
JP600_PIN_8
JP600_PIN_10
JP600_PIN_12
JP600_PIN_14
JP600_PIN_16
JP600_PIN_18
JP600_PIN_20
JP600_PIN_22
I2C_BKLT_SDA
I2C_BKLT_SCL
JP600_PIN_28
JP600_PIN_30
JP600_PIN_32
JP600_PIN_34
JP600_PIN_36
JP600_PIN_38
JP600_PIN_40
JP600_PIN_42
RP611
47K
5%
1/20W
MF
201
MIPI_DATA_CONN_N
MIPI_DATA_CONN_P
MIPI_CLOCK_CONN_N
MIPI_CLOCK_CONN_P
LP602
3.25-OHM-0.1A-2.4GHZ
TAM0605-4SM
MIPI_FTCAM_DATA_ISOL_N
MIPI_FTCAM_DATA_ISOL_P
LP603
3.25-OHM-0.1A-2.4GHZ
TAM0605-4SM
MIPI_FTCAM_CLK_ISOL_N
MIPI_FTCAM_CLK_ISOL_P
VOLTAGE=5V
PP5V_CAM
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
LP610
FERR 120-OHM-1.5A
0402A
CP610
0.1UF
10%
16V
X5R-CERM
0201
107S00116
NO_XNET_CON ECTION=1
RP621
0.1
1%
0.5W
MF
0306
PP5V_SW_LCD
PP5V_SW_LCD_CONN
VOLTAGE=5V
ISNS_PP5V_SW_LCD_P
ISNS_PP5V_SW_LCD_N
PP5V_S2_ALSCAM_ISNS
JP600_PIN_18
JP600_PIN_2
JP600_PIN_8
JP600_PIN_10
JP600_PIN_12
JP600_PIN_14
JP600_PIN_16
DISPLAY:P0
DISPLAY:P1
RP640
RP641
RP642
RP643
RP644
RP645
RP646
RP647
RP648
RP649
UART_TCON_HDMI_D2R
SPI_TCON_CS_L
SPI_TCON_MISO
SPI_TCON_MOSI
SPI_TCON_CLK
RP601
33
SPI_TCON_MOSI_R
RP602
SPI_TCON_CLK_R
RP614
100K
1%
1/20W
MF
201
JP600_PIN_34
JP600_PIN_30
JP600_PIN_36
JP600_PIN_32
JP600_PIN_38
JP600_PIN_40
RP650
RP651
RP652
RP653
RP654
RP655
RP656
RP657
I2C_ALS_1V8_SDA
I2C_ALS_1V8_SCL
I2C_FTCAM_ISOL_SCL
I2C_FTCAM_ISOL_SDA
RP664
RP660
RP661
RP662
RP663
JP600_PIN_20
UART_TCON_HDMI_R2D
I2C_MLB2JERRY_3V3_SDA
I2C_MLB2JERRY_3V3_SCL
TP_TCON_SWCLK
TP_TCON_SWDIO
RP670
RP671
RP672
RP673
RP674
RP675
RP676
RP677
5%
1/20W
MF
0201
BOM_COST_GROUP=DISPLAY
PAGE TITLE
DISPLAY: CONNECTOR, PWR

*** OK2INTEGRATE ***



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PAGE TITLE
DISPLAY POWER SEQUENCER

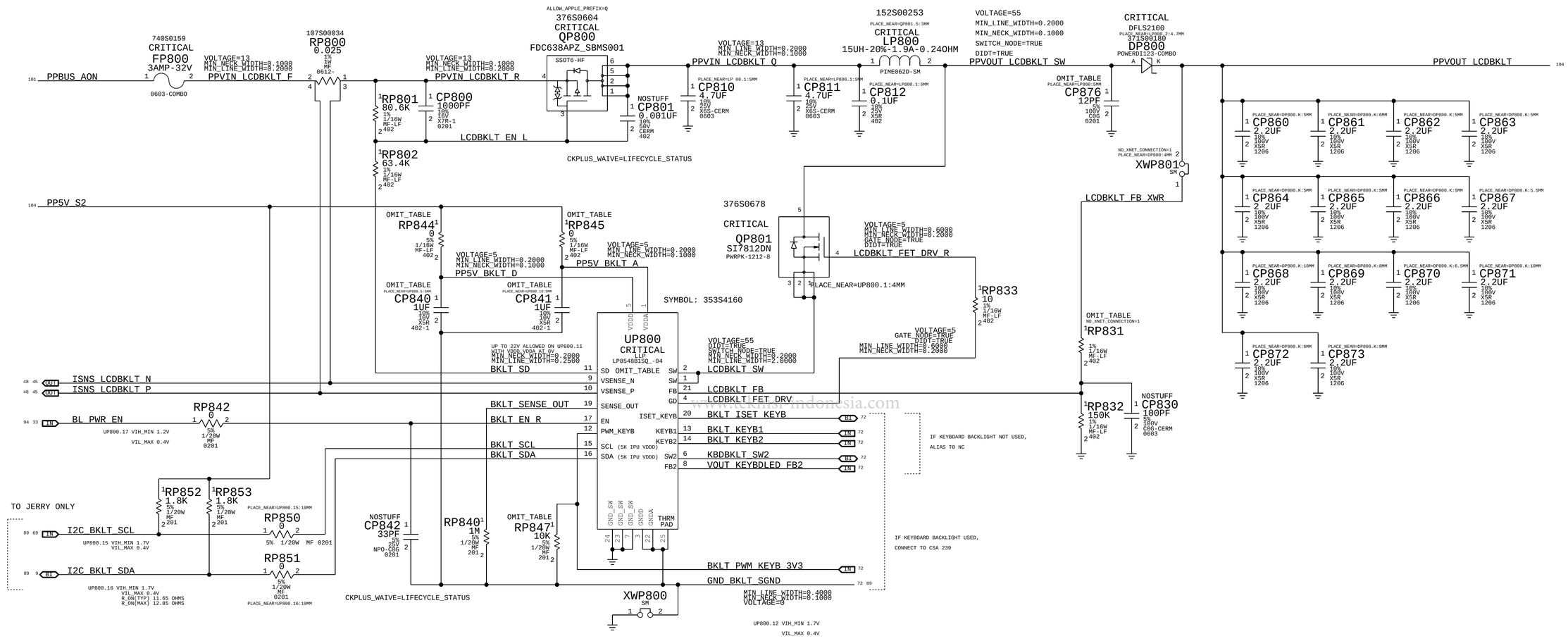
BOM_COST_GROUP=DISPLAY

B

2 1

*** OK2INTEGRATE ***

BEN IC: DISPLAY/KBD BACKLIGHT BOOST CONVERTER



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BEN IC VERSION TO MATCH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4160	1	IC,LP8548B1-04,DC/DC CVTR,BOOST,QFN-24	UP800		BLC_BEN_IC:V4
353S02256	1	IC,LP8548B1A-07,DC/DC BOOST CVTR,QFN24	UP800		BLC_BEN_IC:V7

BACKLIGHT SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CP876		BLC_SW_NODE_DESENSE

10K IF KEYBOARD PWM INPUT IS NOT PRESENT (J132, J213)
100K IF KEYBOARD PWM INPUT IS PRESENT (J152)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0007	1	RES,MF,1/20W,10K OHM,5,0201,SMD	RP847		BLC_KBD_BOOST_USED:NO
118S0014	1	RES,MF,100KOHM,1,1/20W,0201	RP847		BLC_KBD_BOOST_USED:YES

BACKLIGHT BOOST VOLTAGE LEVEL BASED ON NUMBER OF LEDS PER STRING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0339	1	RES,MTL FILM,1/16W,18.2K,1,0402,SM,LF	RP831		BLC_LEDS_PER_STRING:16
114S0359	1	RES,MTL FILM,1/16W,28.7K,1,0402,SM,LF	RP831		BLC_LEDS_PER_STRING:18

BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION,
AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR://50602542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	RP844,RP845		BLC_5V_SERIES:0_OHM
114S0023	2	RES,MTL FILM,1/16W,10 OHM,1,0402,SMD,LF	RP844,RP845		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CP840,CP841		BLC_5V_CAP:1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CP840,CP841		BLC_5V_CAP:4P7_UF

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=REF_BLC_BEN SYNC_DATE=11/21/2019

PAGE TITLE

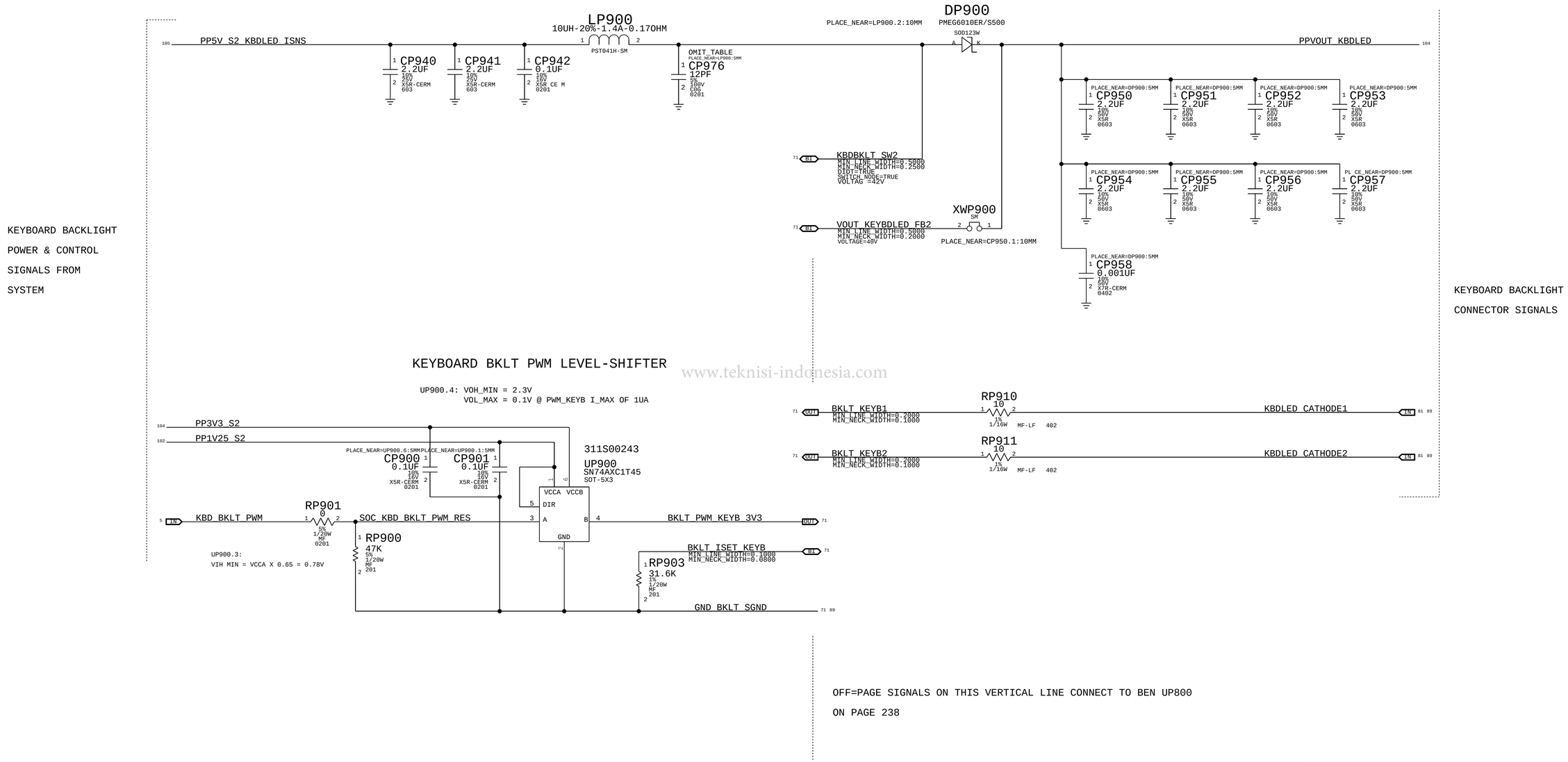
BEN: CONTROLLER

8 6 2 1

*** OK2INTEGRATE ***

BEN IC: KEYBOARD LED DRIVER

THIS PAGE IS ONLY TO BE INCLUDED IF THE KEYBOARD BACKLIGHT
IS CONTROLLED BY THE BEN ON PAGE 238



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OFF=PAGE SIGNALS ON THIS VERTICAL LINE CONNECT TO BEN UP800
ON PAGE 238

KEYBOARD SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CP976		BLC_KBD_SW_NODE_DESENSE

BOM_COST_GROUP=DISPLAY

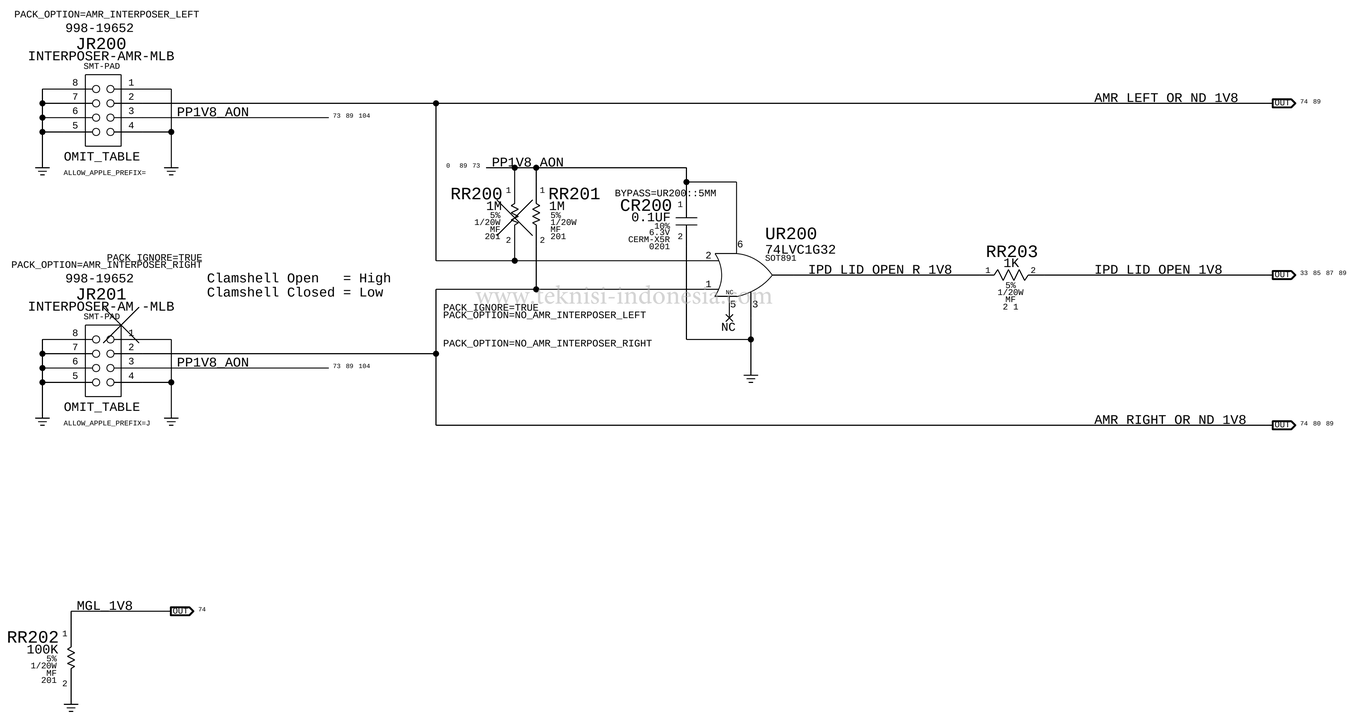
SYNC_MASTER=REF_BLC_BEN SYNC_DATE=11/21/2019

PAGE TITLE

BEN: KEYBOARD

*** OK2INTEGRATE ***

Lid Detect Sensors



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PAGE TITLE

SECDIS: AMR

BOM_COST_GROUP=SOC

*** OK2INTEGRATE ***

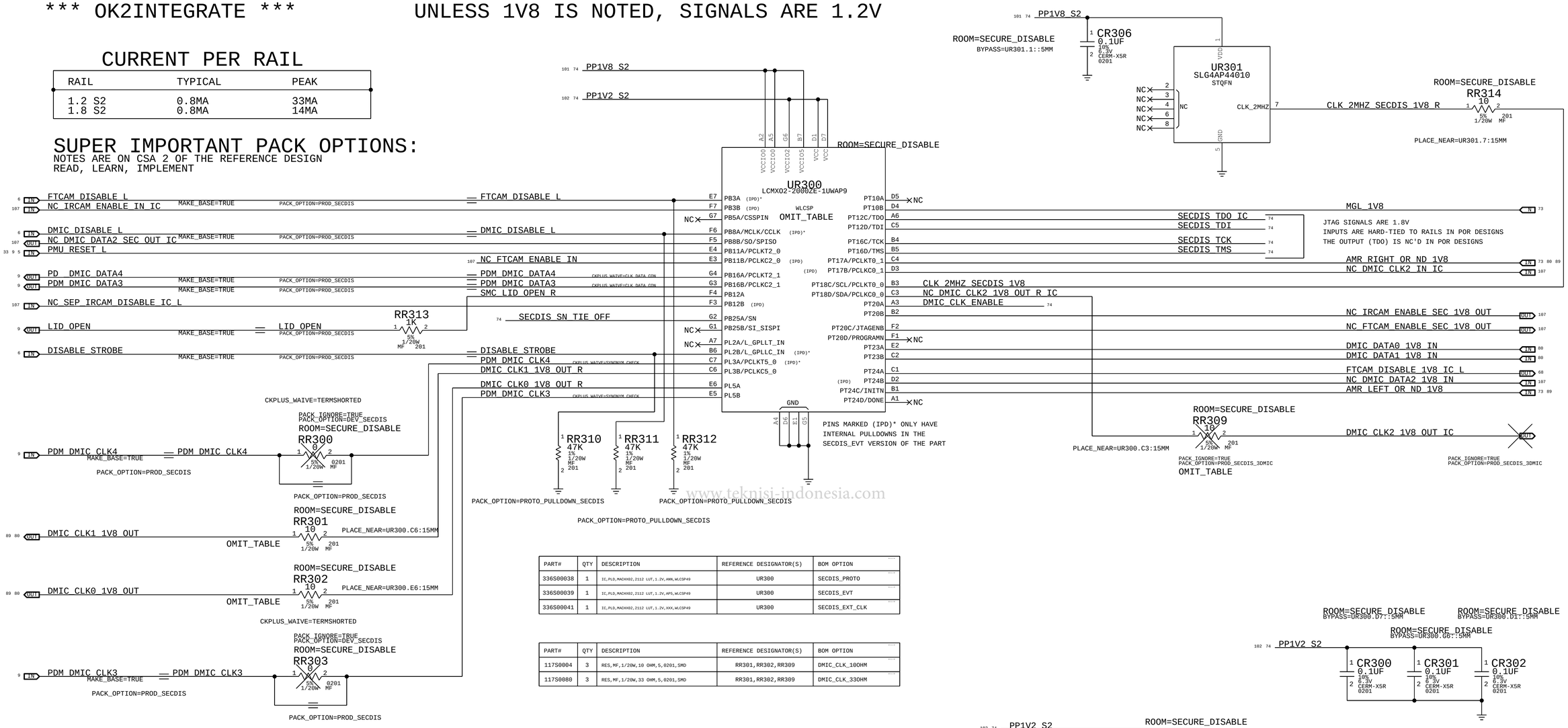
UNLESS 1V8 IS NOTED, SIGNALS ARE 1.2V

CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	0.8MA	33MA
1.8 S2	0.8MA	14MA

SUPER IMPORTANT PACK OPTIONS:

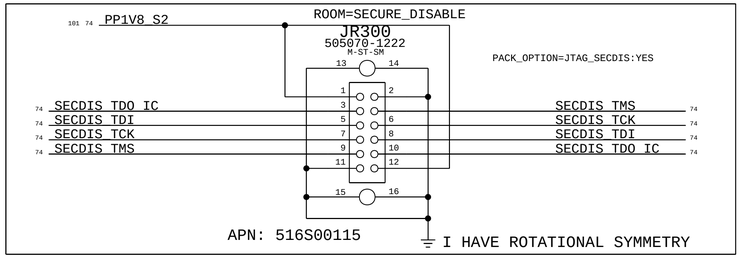
NOTES ARE ON CSA 2 OF THE REFERENCE DESIGN
READ, LEARN, IMPLEMENT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
336S00038	1	IC,PLD,MACHX02,2112 LUT,1.2V,ANN,WLCSP49	UR300	SECDIS_PROTO
336S00039	1	IC,PLD,MACHX02,2112 LUT,1.2V,APS,WLCSP49	UR300	SECDIS_EVT
336S00041	1	IC,PLD,MACHX02,2112 LUT,1.2V,XXX,WLCSP49	UR300	SECDIS_EXT_CLK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0004	3	RES,MF,1/20W,10 OHM,5,0201,SMD	RR301,RR302,RR309	DMIC_CLK_10OHM
117S0080	3	RES,MF,1/20W,33 OHM,5,0201,SMD	RR301,RR302,RR309	DMIC_CLK_33OHM

JTAG FOR DEV & PROTO0 BOARDS ONLY



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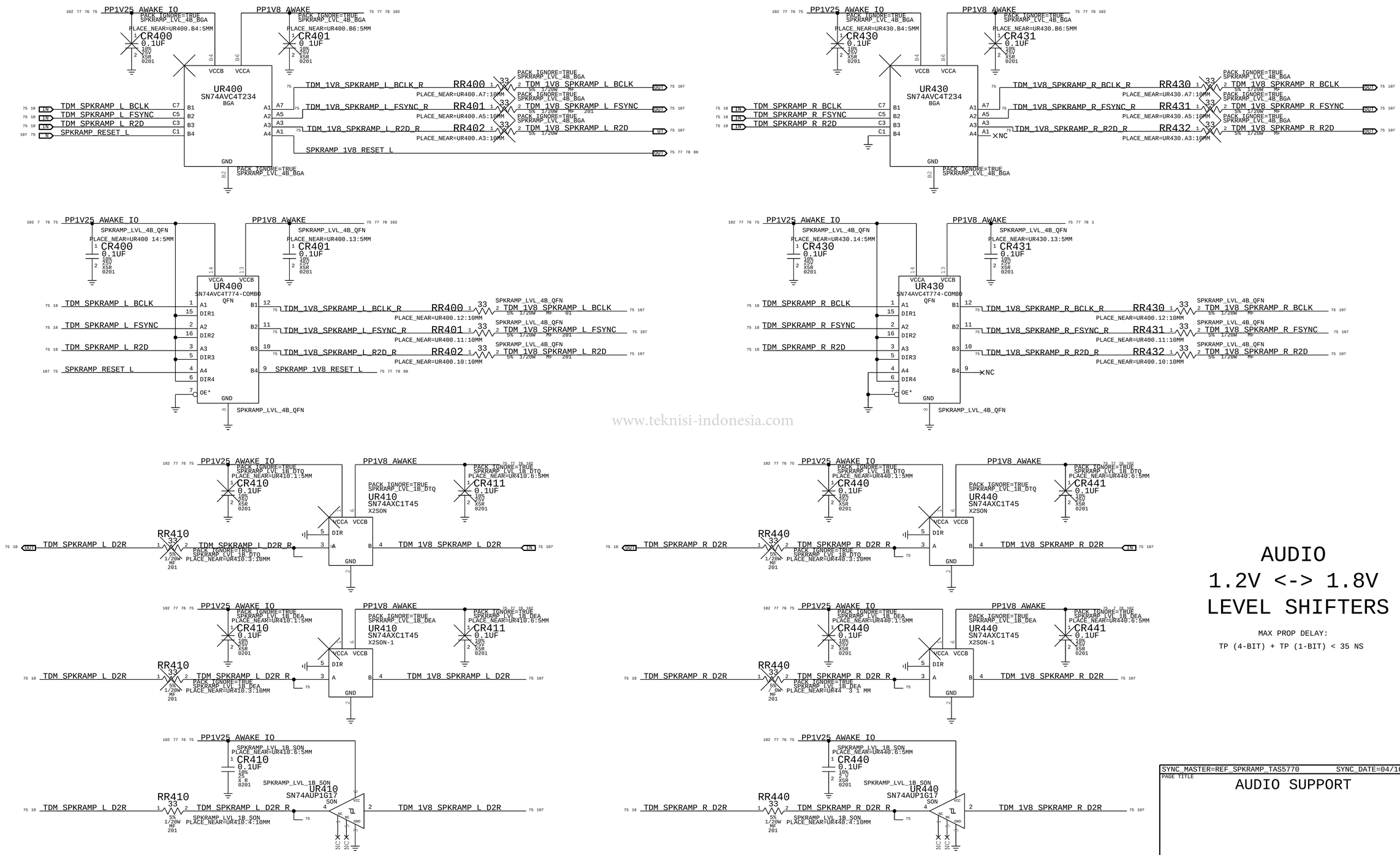
*** OK2INTEGRATE ***



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AUDIO
1.2V <-> 1.8V
LEVEL SHIFTERS

MAX PROP DELAY:

TP (4-BIT) + TP (1-BIT) < 35 NS

SYNC_MASTER=REF_SPKRAMP_TAS5770 SYNC_DATE=04/16/2020

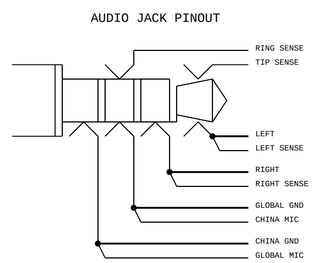
PAGE TITLE

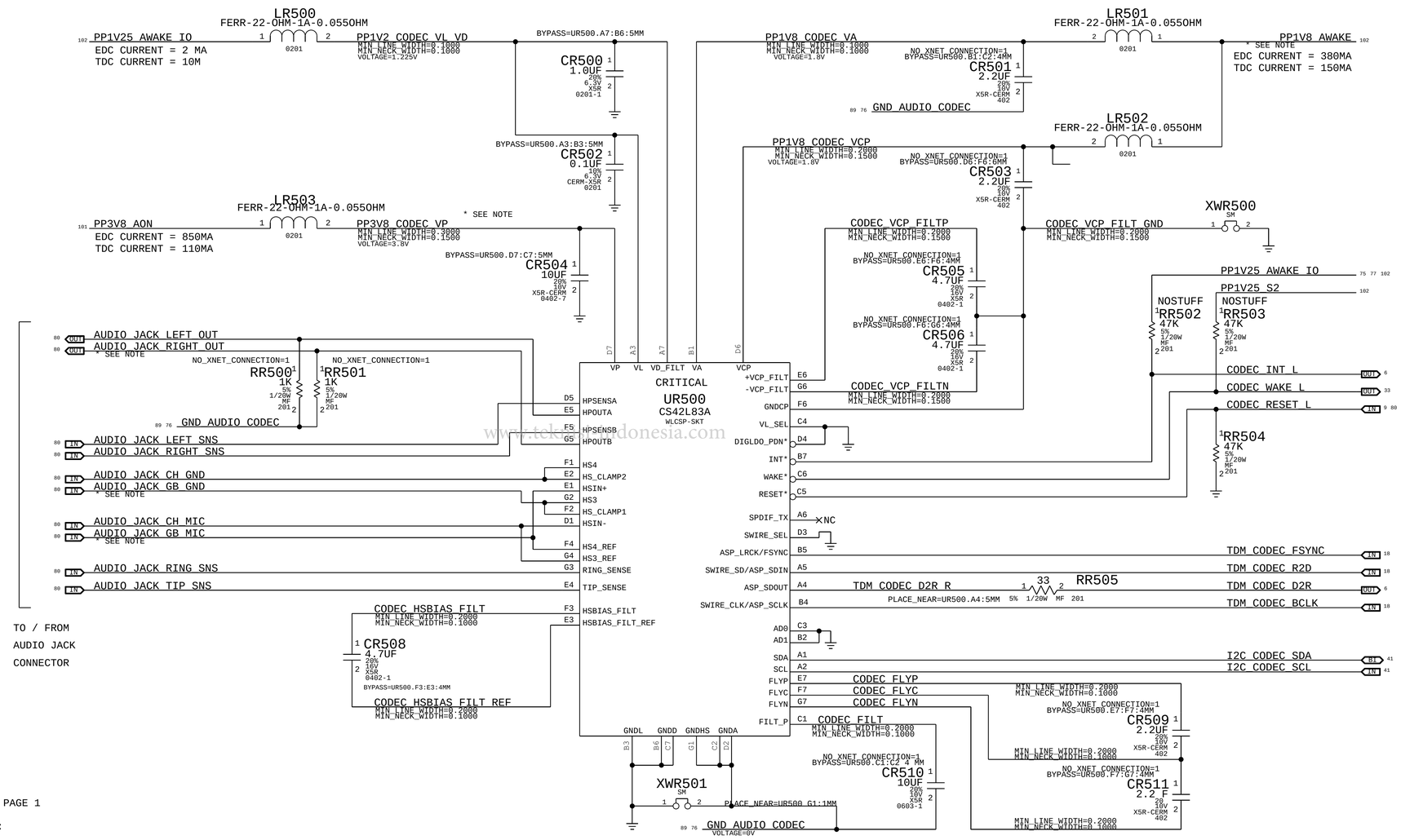
AUDIO SUPPORT

*** OK2INTEGRATE ***

AUDIO JACK CODEC I2C ADDRESS		
AD1	AD0	ADDRESS
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B

CHANGES FROM PREVIOUS DESIGNS:
- REMOVED LDO TO GENERATE LOCAL 1.8V <RDAR://50645294>
- CHANGED VL SUPPLY FROM 1.8V TO 1.2V <RDAR://TBD>
- SUPPLIED VD_FILT EXTERNALLY <RDAR://TBD>
- CHANGED VP SUPPLY FROM 3.3V TO 3.8V <RDAR://TBD>





NOTES:

- SEE TEST POINT SIGNALS & LOCATIONS ON REF DESIGN PAGE 1

- THE FOLLOWING SIGNALS SHOULD HAVE A LOW DCR PATH:
  - VP SUPPLY
  - VCP SUPPLY
  - AUDIO_JACK_LEFT/RIGHT_OUT
  - AUDIO_JACK_GB/CH_GND

- GB_MIC SIGNAL CONNECTS TO CH_GND AT A/J CONNECTOR.
  CH_MIC SIGNAL CONNECTS TO GB_GND AT A/J CONNECTOR.

- VP SUPPLY RAIL ACCEPTS 3.0V TO 5.25V AND NEEDS TO COME UP FIRST AND TURN OFF LAST (NEED TO STAY UP WHEN THE OTHER RAILS GO DOWN)
  VP CURRENT CONSUMPTION WITH PART IN LOWEST POWER STATE:
  3.1UA (1V8 OFF, RST# LOW)
  3.6UA (1V8 ON, RST# LOW)
  36UA (1V8 ON, RST# HIGH)

SYNC_MASTER=REF_CODEC_CLIFDEN

PAGE TITLE

AUDIO JACK CODEC

BOM_COST_GROUP=AUDIO

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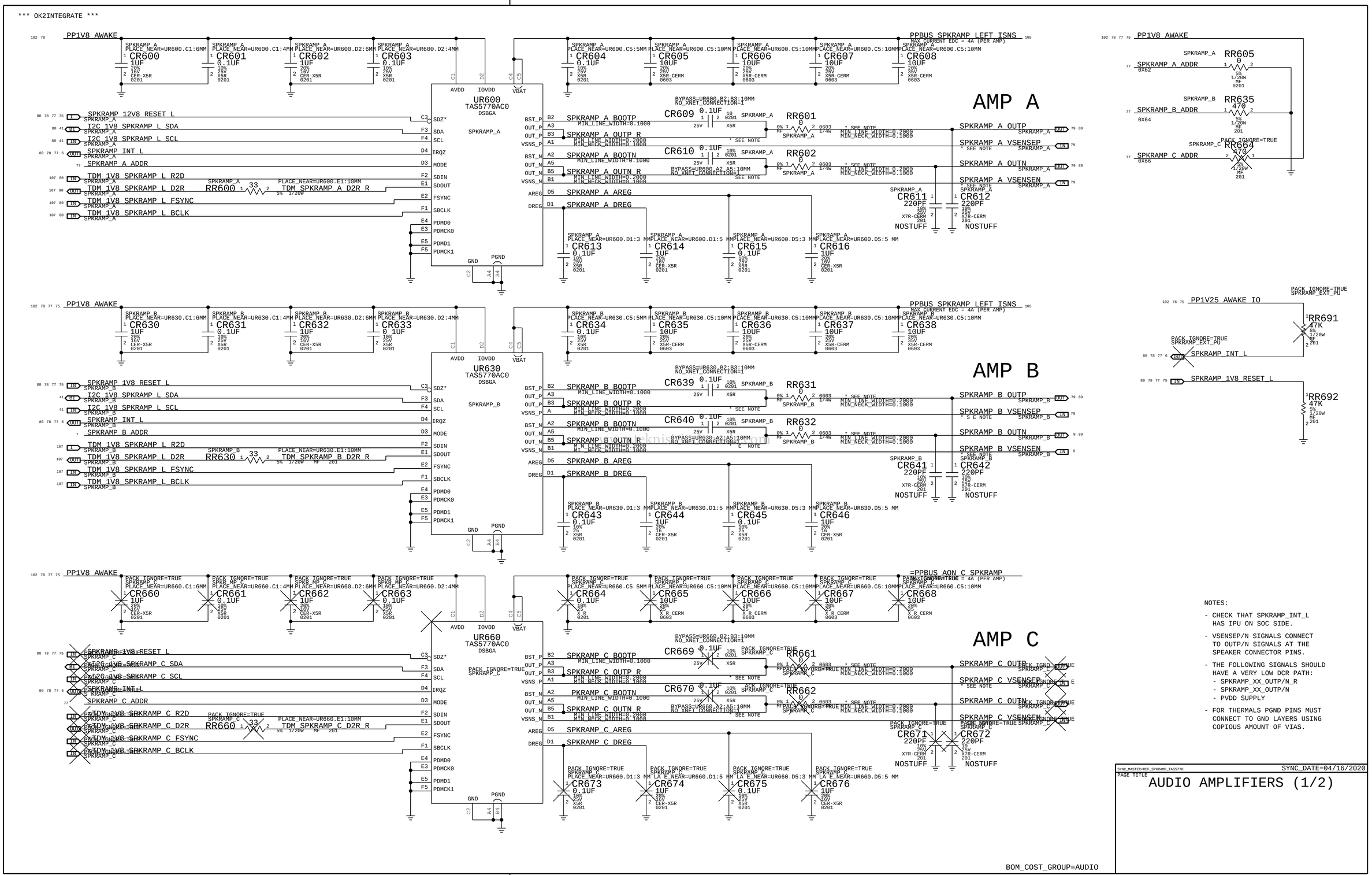


NOTES:

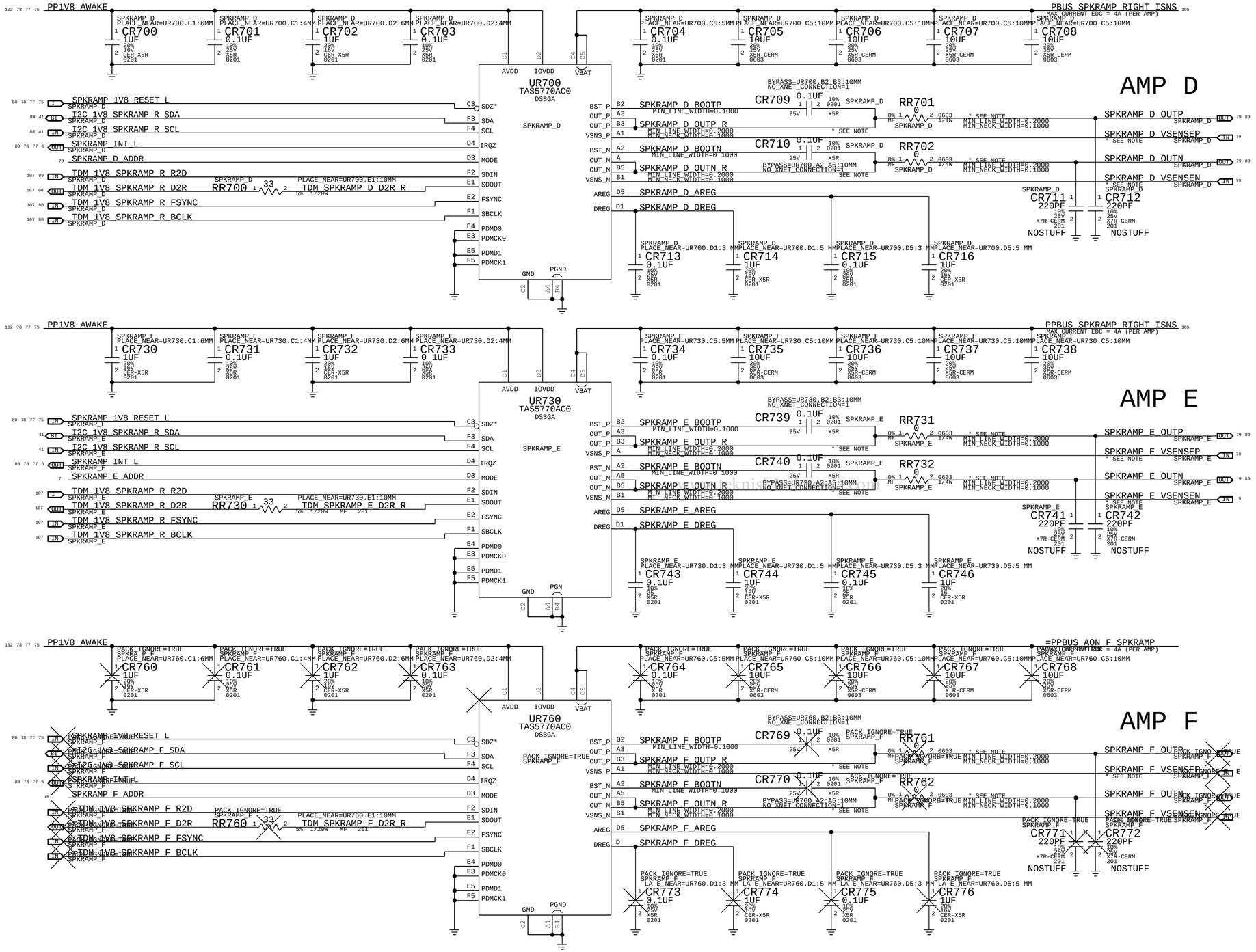
- CHECK THAT SPKRAMP_INT_L HAS IPU ON SOC SIDE.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.

SYNC_MASTER=REF_SPKRAMP_TAS5770 SYNC_DATE=04/16/2020

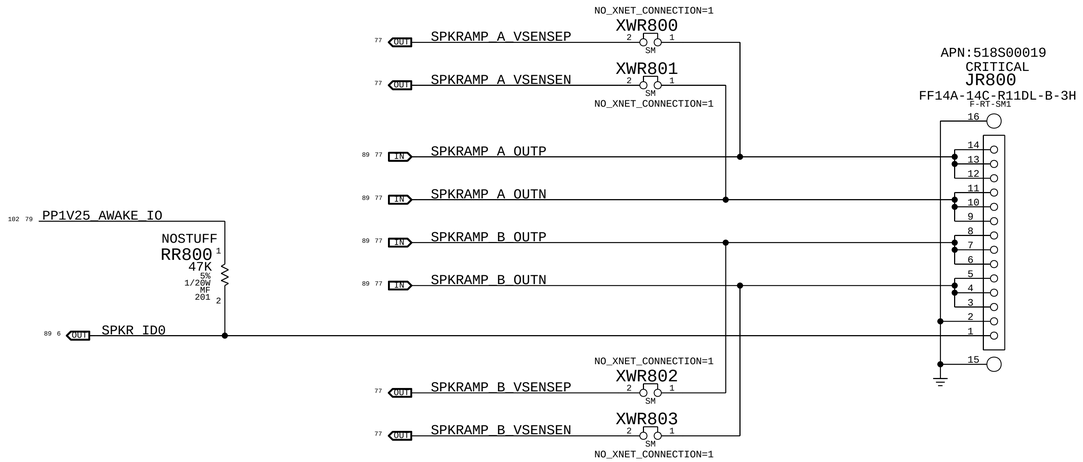
PAGE TITLE

AUDIO AMPLIFIERS (1/2)

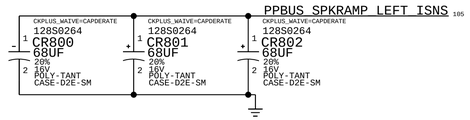
*** OK2INTEGRATE ***



LEFT AUDIO AMP CONNECTOR



LEFT AUDIO AMP PBUS BULK CAPS



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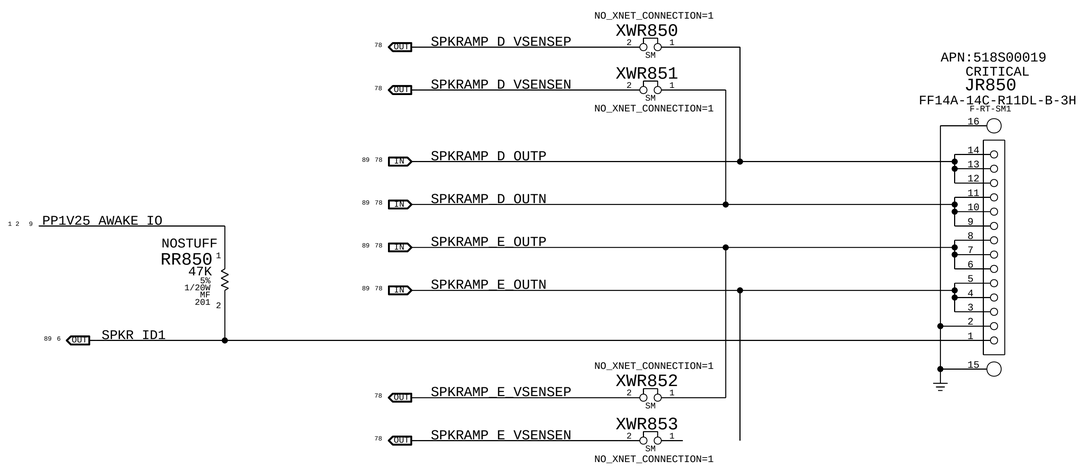
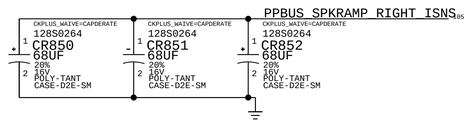
RIGHT AUDIO AMP CONNECTOR



RIGHT AUDIO AMP PBUS BULK CAPS



SYNC_MASTER=KELVIN T668_MLB

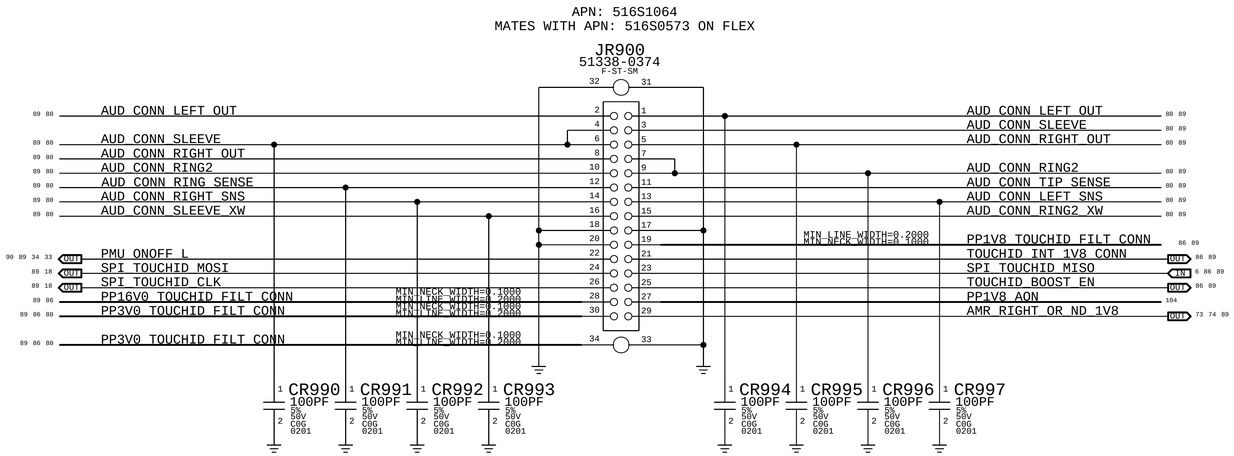
PAGE TITLE

AUDIO CONNECTORS: AMPS

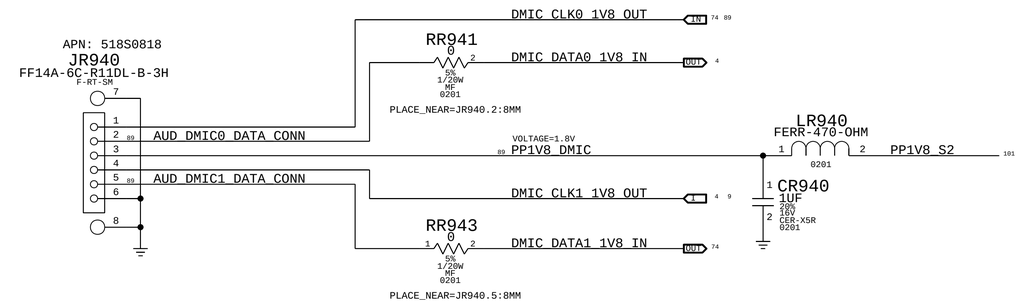
A

BOM_COST_GROUP=AUDIO

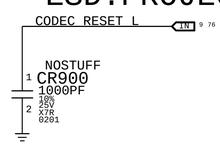
AUDIO JACK FLEX CONNECTOR



DIGITAL MIC FLEX CONNECTOR



ESD:PROJECT DEPENDENT



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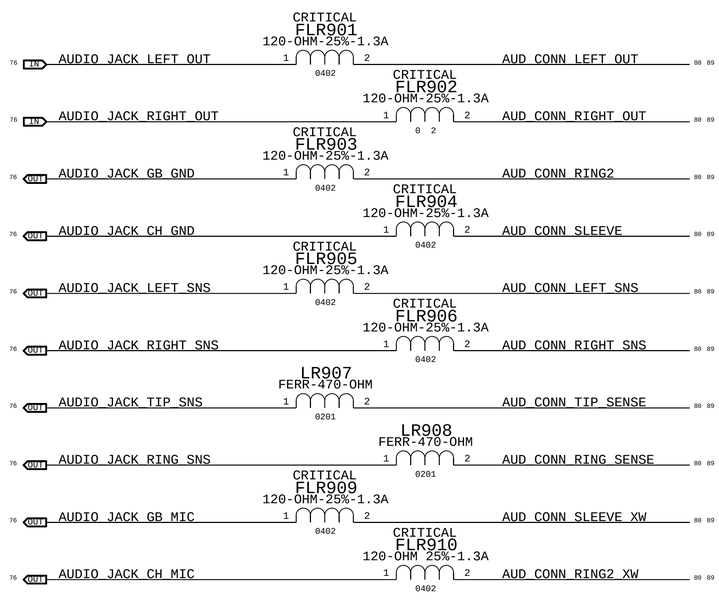
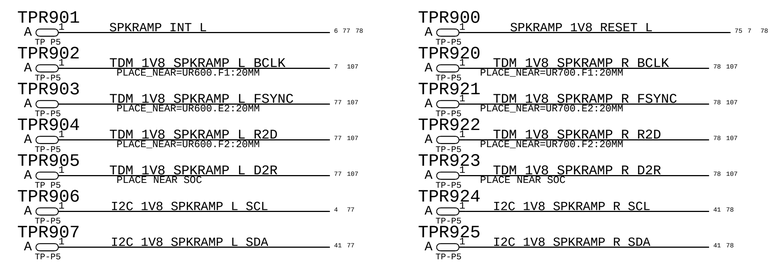


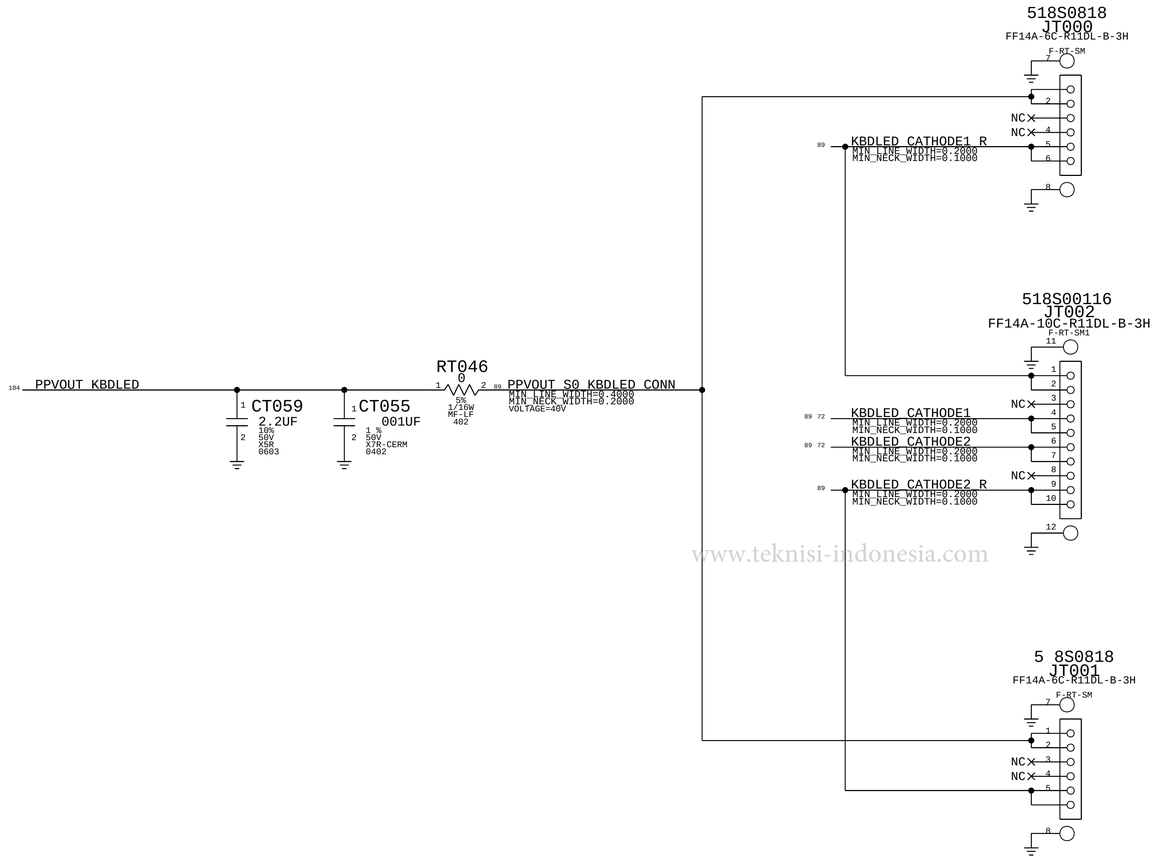


BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO CONNECTORS: DMIC, JACK

A

2 1



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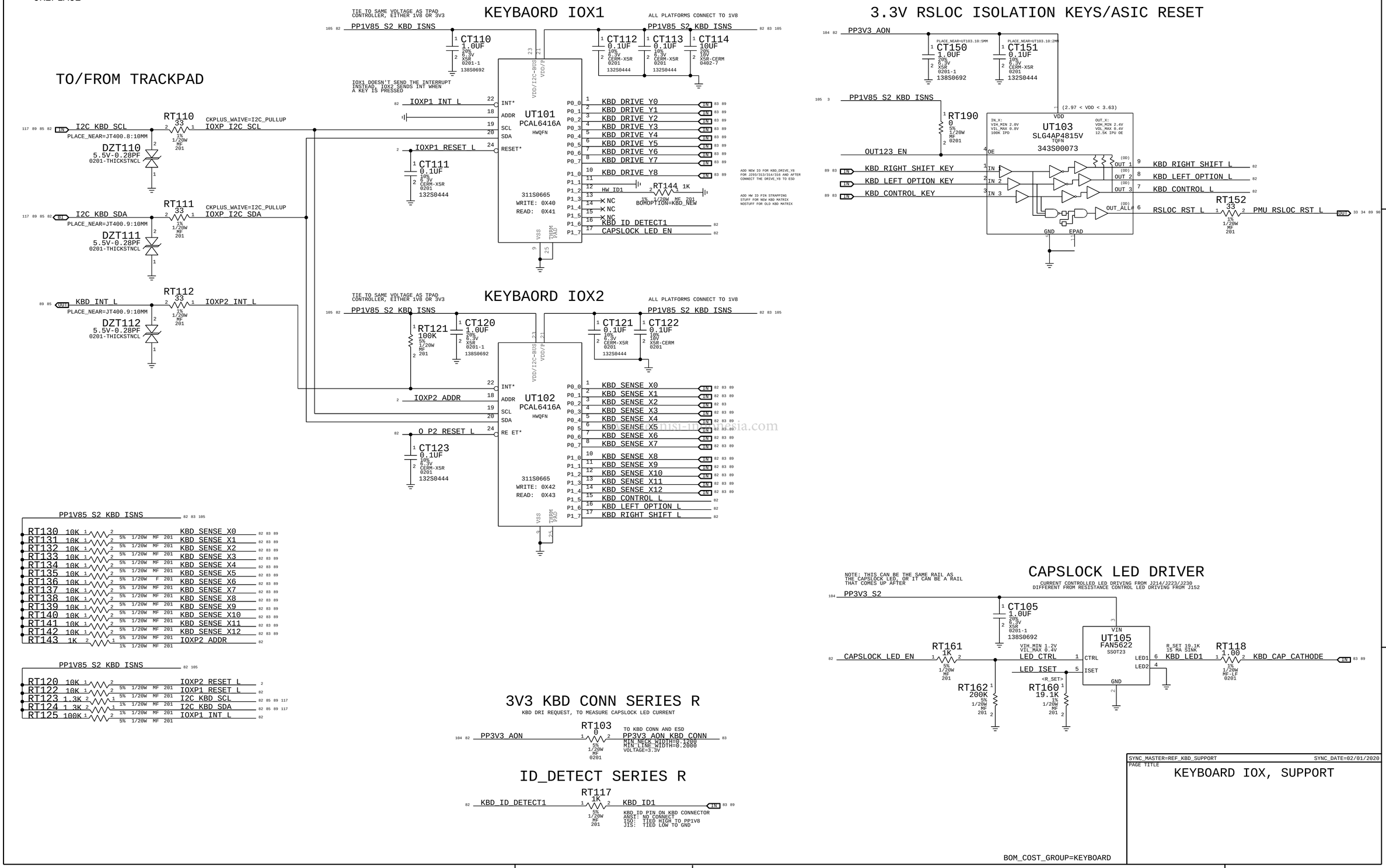
SYNC_MASTER=T668_MLB SYNC_DATE=05/16/2019

PAGE TITLE

KEYBOARD BLC CONNECTORS

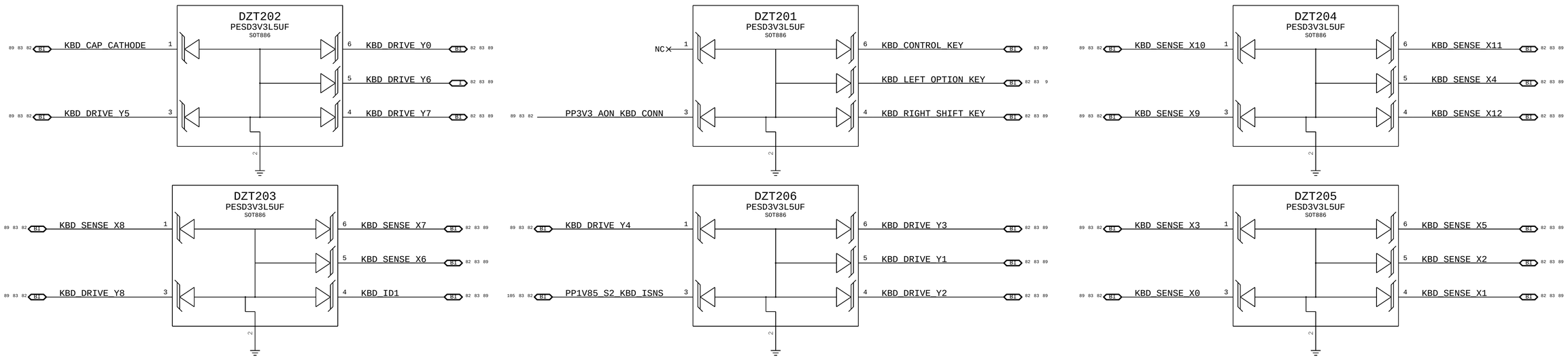
BOM_COST_GROUP=DISPLAY

*** OK2PLACE ***



kamisi-indonesia.com

KEYBOARD ESD



MEMBRANE ZIF CONNECTOR

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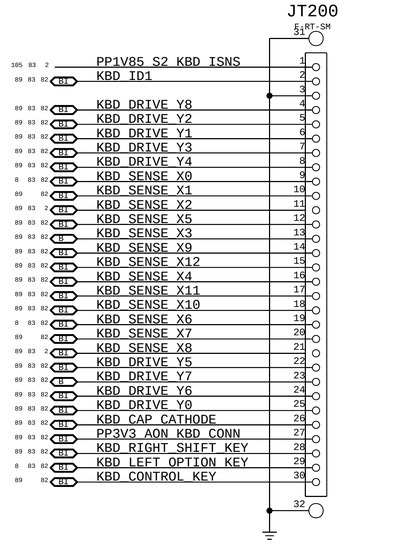
518S0752
CRITICAL
FF14A-30C-R11DL-B-3H

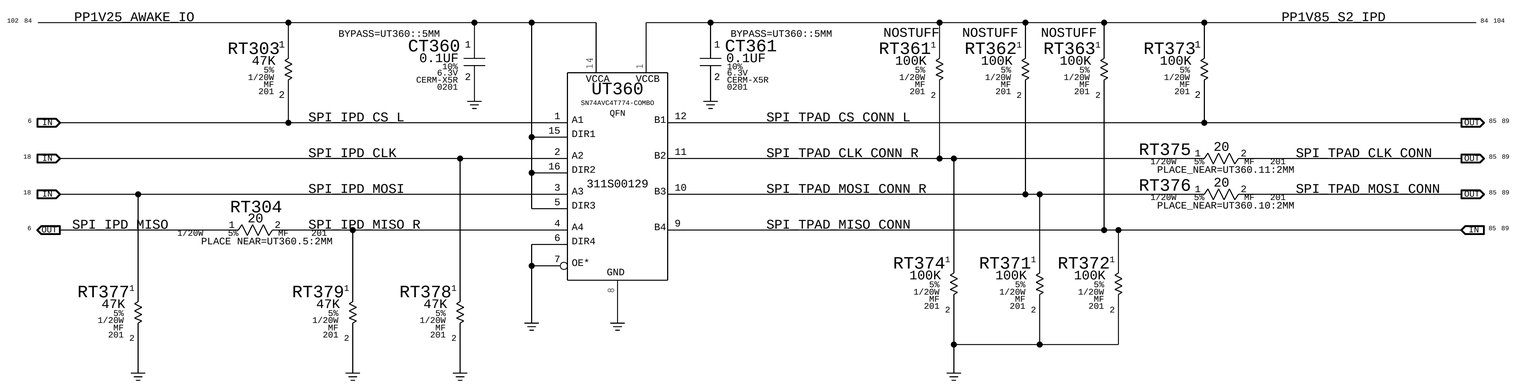


SYNC_MASTER=WUDI_T668_MLB SYNC_DATE=01/28/2020

PAGE TITLE
KEYBOARD SIGNAL CONNECTOR, ESD

BOM_COST_GROUP=KEYBOARD

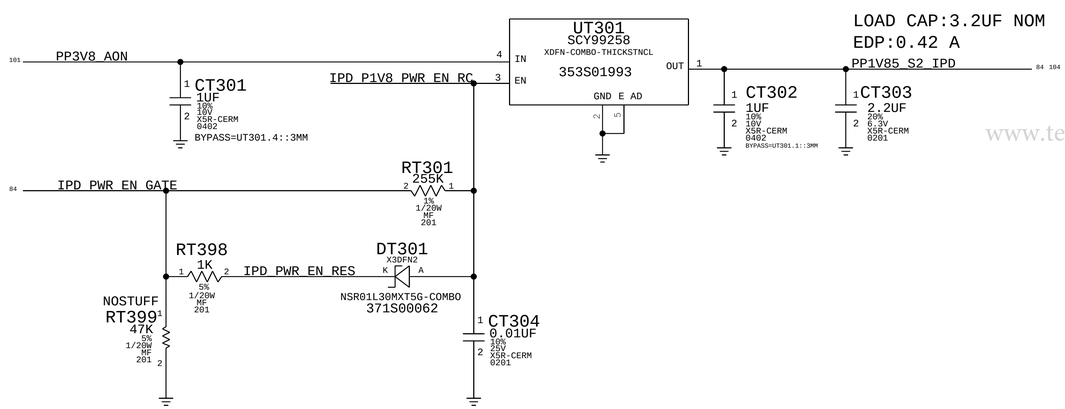
TRACKPAD SPI BUS LEVEL SHIFTER (+1.2V TO +1.8V)



SN74AVC4T774 Truth Table

CTRL INPUTS		OUTPUT CIRCUITS		OPERATION
/OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

IPD LDO
1.85 V FOR TRACKPAD AND KEYBOARD IOX



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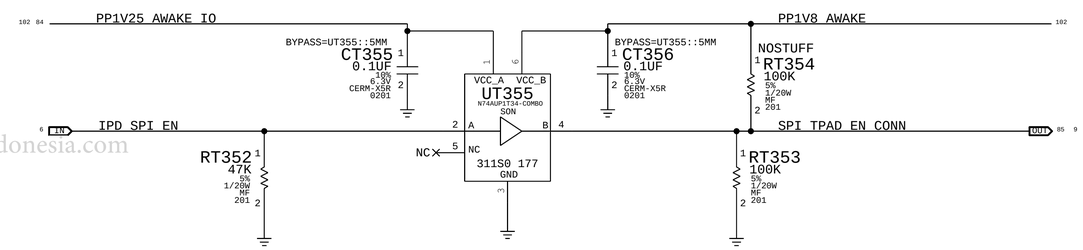
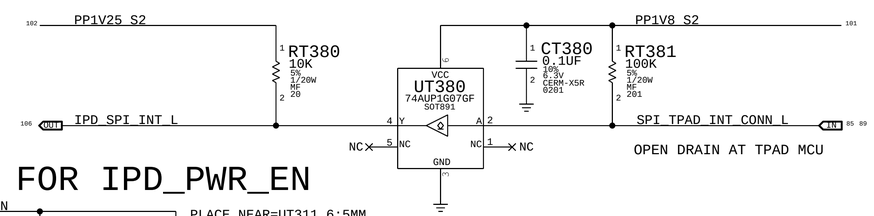
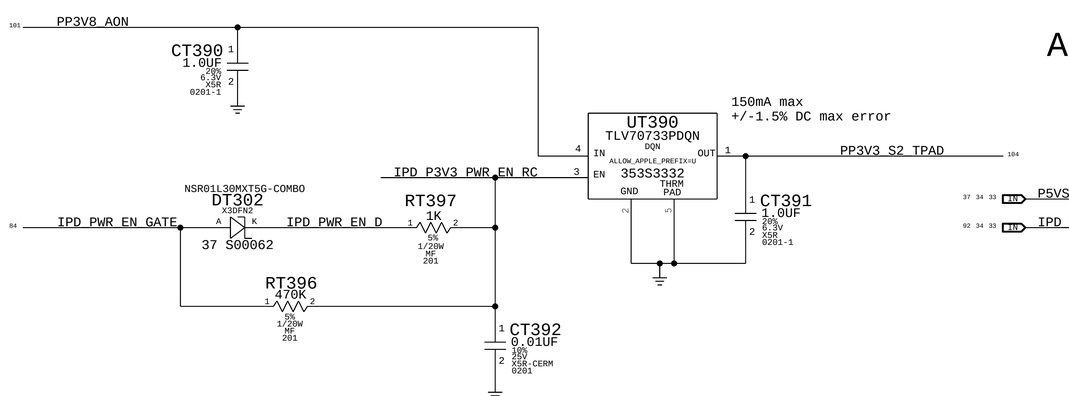
TRACKPAD SPI ENABLE LEVEL SHIFTER



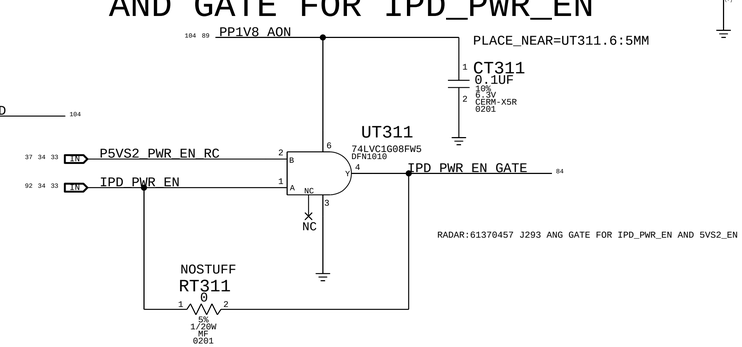
IPD SPI INTERRUPT LEVEL SHIFTER



3.3V S2 LDO FOR TPAD



AND GATE FOR IPD_PWR_EN



RADAR:61370457 J293 ANG GATE FOR IPD_PWR_EN AND 5VS2_EN

BOM_COST_GROUP=TRACKPAD

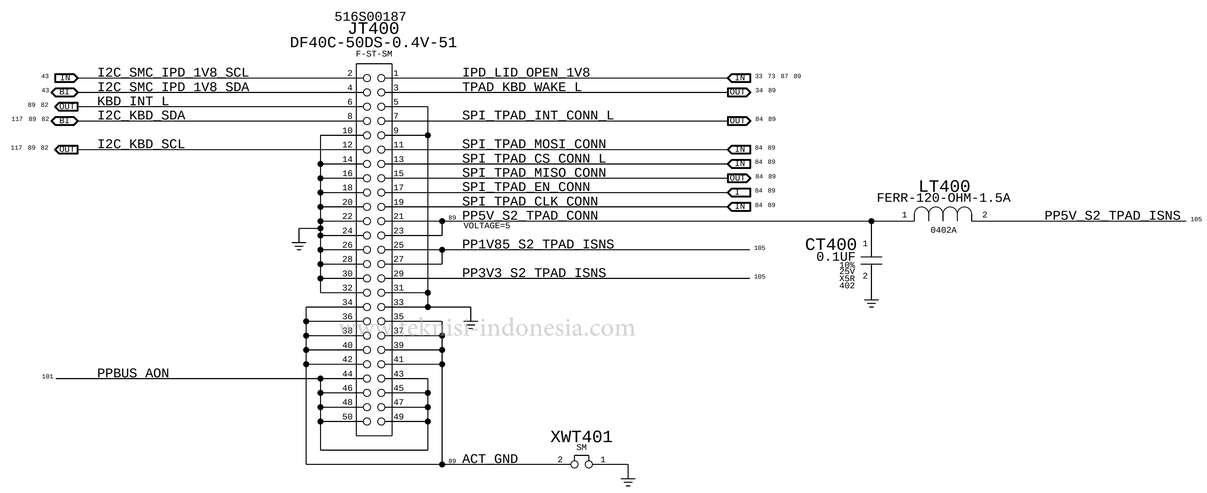
SYNC_MASTER=MODI_T668_MLB SYNC_DATE=04/16/2020

PAGE TITLE

TRACKPAD SUPPORT

2 1

MATES WITH 518S00080 ON TRACKPAD FLEX



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BOM_COST_GROUP=TRACKPAD

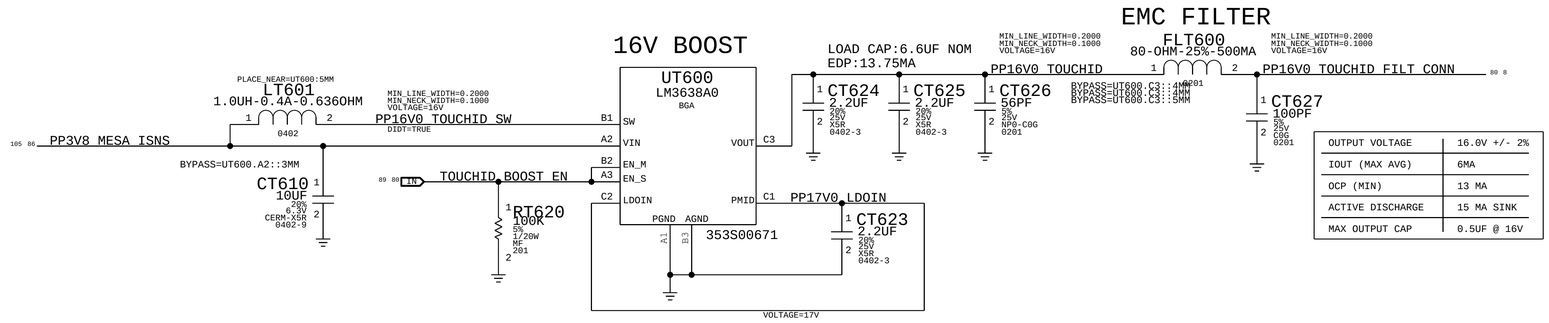
SYNC_MASTER=WGOI_T668_MLB SYNC_DATE=04/16/2020

PAGE TITLE

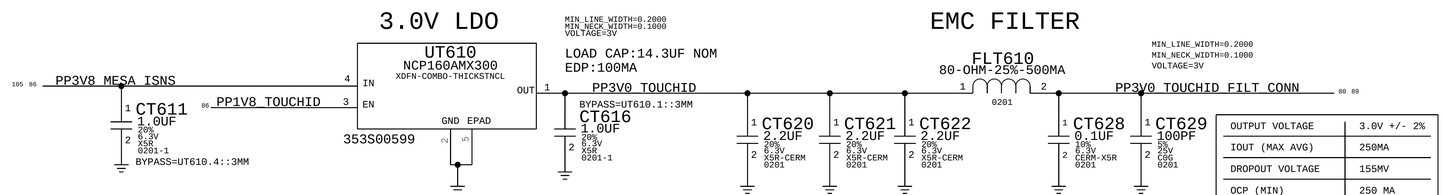
TRACKPAD CONNECTOR

*** OK2INTEGRATE ***

TOUCHID POWER SEQUENCING REQUIREMENTS
POWER ON: 1V8 -> 3V3 -> 16V0



OUTPUT VOLTAGE	16.0V +/- 2%
IOUT (MAX AVG)	6MA
OCP (MIN)	13 MA
ACTIVE DISCHARGE	15 MA SINK
MAX OUTPUT CAP	0.5UF @ 16V



OUTPUT VOLTAGE	3.0V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	155MV
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP

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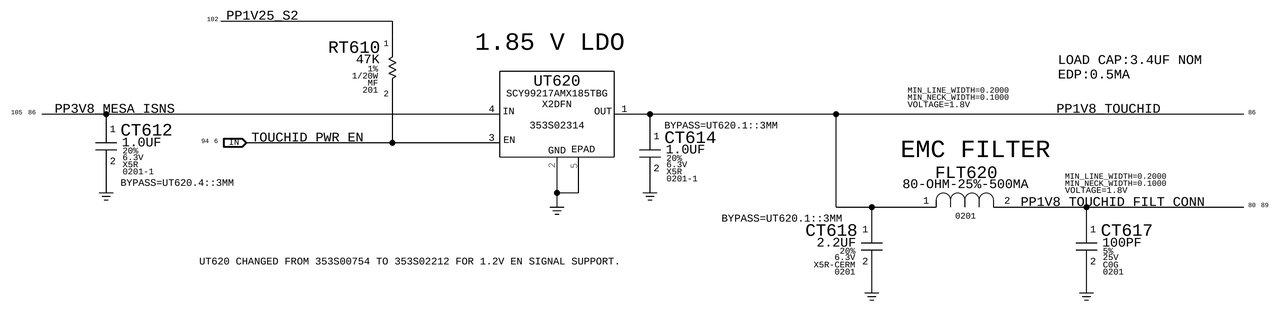
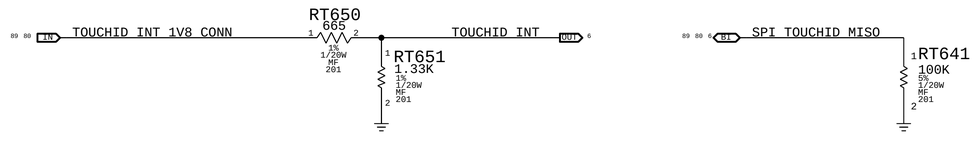


UT620 CHANGED FROM 353S00754 TO 353S02212 FOR 1.2V EN SIGNAL SUPPORT.

OUTPUT VOLTAGE	1.825 V +/- 2%
IOUT (MAX AVG)	250 MA
DROPOUT VOLTAGE	75MV TYP @ 100MA
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MIN OUTPUT CAP	1.0 UF



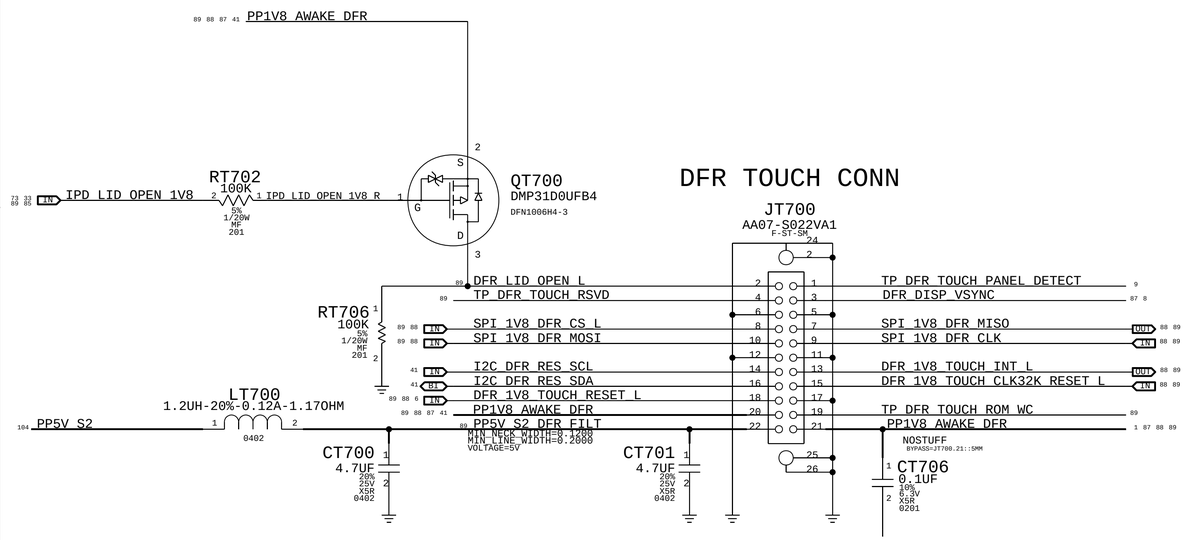
BOM_COST_GROUP=TOUCH ID

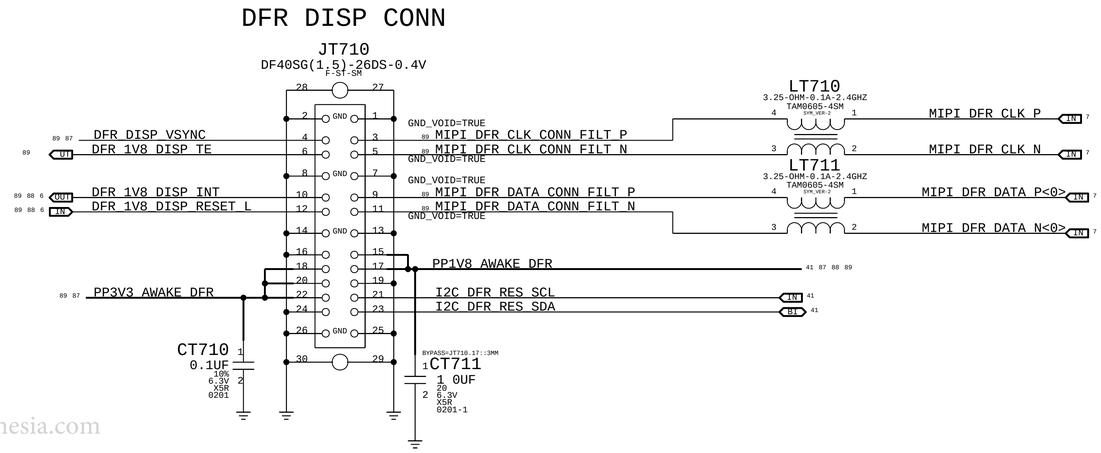
PAGE TITLE
TOUCHID SUPPORT

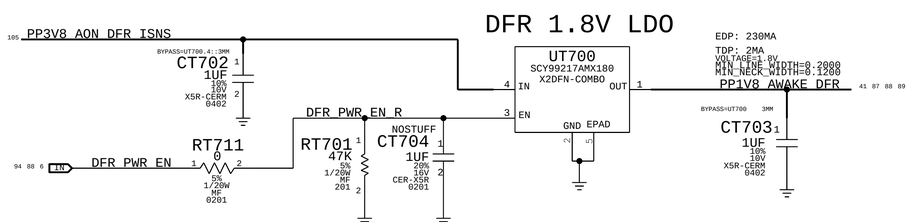
A

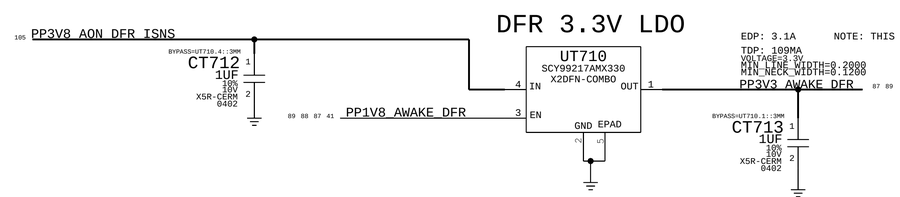
OK2INTEGRATE

DFR V3 SUPPORT









NOTE: THIS IS INRUSH CURRENT SPEC ONLY.THE LDO WILL CURRENT LIMIT THIS VALUE.

OUTPUT VOLTAGE	1.8V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	80MV TYP @ 250MA
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MAX OUTPUT CAP	

OUTPUT VOLTAGE	3.3V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	80MV TYP @ 250MA
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MAX OUTPUT CAP	

BOM_COST_GROUP=TOUCH BAR

PAGE TITLE

DFR SUPPORT 1

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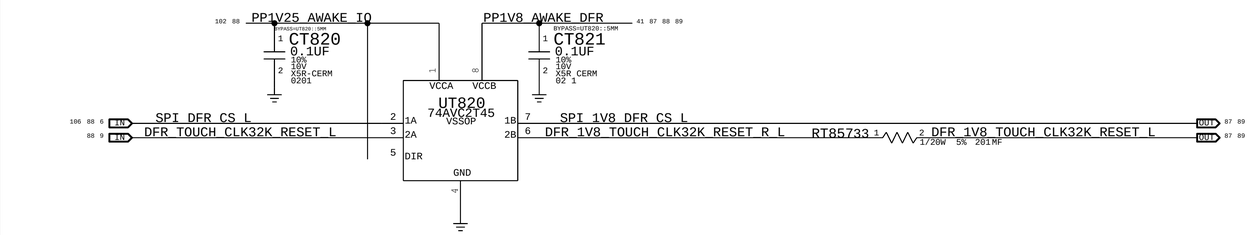
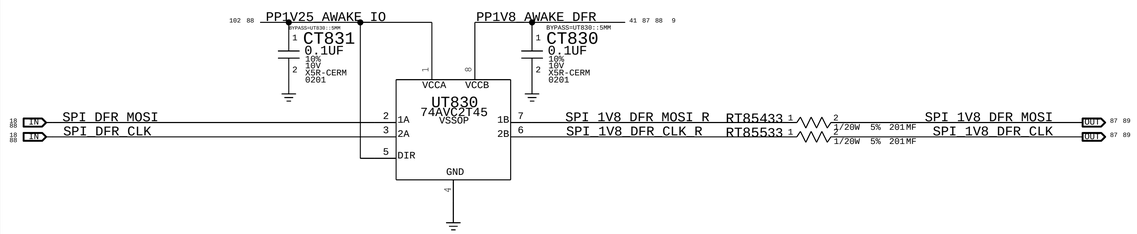
OK2INTEGRATE

DFR V3 SUPPORT





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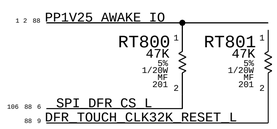

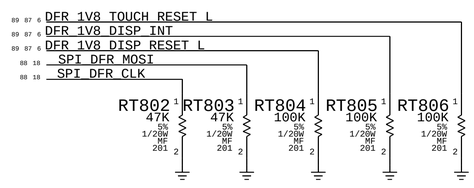

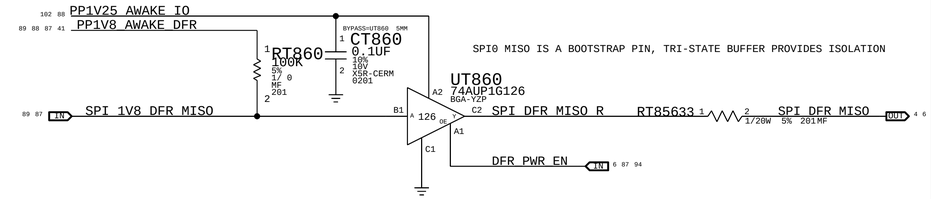

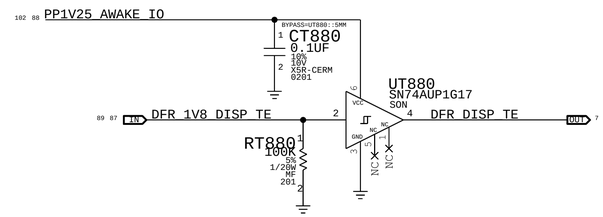

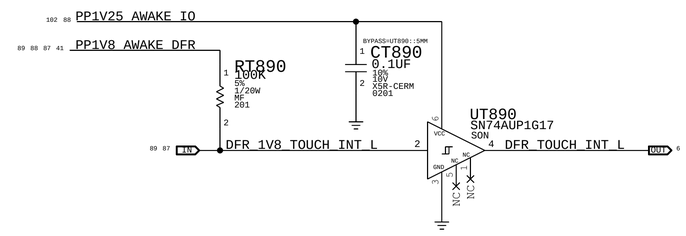

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18	EUSB ATC0 R P	TPU600	TP-P5
18	EUSB ATC0 R N	TPU601	TP-P5
90 56 33 5	SOC FORCE DFU	TPU602	TP-P5
94 56 19 5	SOC DFU STATUS	TPU603	TP-P5
56 18 6	UART DEBUGPRT R2D	TPU604	TP-P5
56 18 6	UART DEBUGPRT D2R	TPU605	TP-P5
56 18 9	SWD SOC SWCLK	TPU606	TP-P5
56 18 9	SWD SOC SWDIO	TPU607	TP-P5
56 9	UART SMC DEBUGPRT R2D	TPU608	TP-P5
56 9	UART SMC DEBUGPRT D2R	TPU609	TP-P5
106	TP SOC AMUX OUT	TPU610	TP-P5
18 9	SMC FIXTURE MODE L	TPU611	TP-P5
43 9	I2C SMC UPC SDA	TPU612	TP-P5
43 9	I2C SMC UPC SCL	TPU613	TP-P5
107 100 67 33	PMU SYS ALIVE	TPU614	TP-P5
94 55 33 5	PMU ACTIVE READY	TPU615	TP-P5
90 80 34 33	PMU ONOFF L	TPU616	TP-P5
90 82 34 33	PMU RSLOC RST L	TPU617	TP-P5
100 96 91 33 6	SOC SOCHOT L	TPU618	TP-P5
100 90 74 33 9 5	PMU RESET L	TPU619	TP-P5
90 33	PMU SHDN	TPU620	TP-P5
96 56	USB DBG LS N	TPU634	TP-P5
96 56	USB DBG LS P	TPU635	TP-P5
91 61 57	USB2 UPC0 P1 N	TPU636	TP-P5
91 61 57	USB2 UPC0 P1 P	TPU637	TP-P5

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101	PPVBAT AON	TPU621	TP-P5
		TPU622	TP-P5
		TPU623	TP-P5
		TPU624	TP-P5
		TPU625	TP-P5
		TPU626	TP-P5
		TPU627	TP-P5
		TPU628	TP-P5
43	I2C SMC PWR 3V3 SCL	TPU629	TP-P5
43	I2C SMC PWR 3V3 SDA	TPU630	TP-P5
21	SYS DETECT L	TPU631	TP-P5
21	SYS DETECT	TPU632	TP-P5
	GND	TPU633	TP-P5

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101	PPDCIN USBC AON	TPU640	TP-P5
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		TPU642	TP-P5
		TPU643	TP-P5
		TPU644	TP-P5
		TPU645	TP-P5
98 22	PPDCIN AON CHGR R	TPU646	TP-P5
	GND	TPU647	TP-P5

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52	PP5V S2 TO FAN	TPU650	TP-P5
		TPU651	TP-P5
52	FAN RT PWM	TPU652	TP-P5
52	FAN RT TACH	TPU653	TP-P5
52	TP FAN RT OTP1	TPU654	TP-P5
52	TP FAN RT OTP2	TPU655	TP-P5
52	GND FAN	TPU656	TP-P5
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59 57 55	PPVBUS USBC0	TPU660	TP-P5
		TPU661	TP-P5
		TPU662	TP-P5
		TPU663	TP-P5
59 57	USBC0 SBU1	TPU664	TP-P5
59 57	USBC0 SBU2	TPU665	TP-P5
59 57 56	USBC0 CC1	TPU666	TP-P5
59 57 56	USBC0 CC2	TPU667	TP-P5
	GND	TPU668	TP-P5
59 58 55	PPVBUS USBC1	TPU669	TP-P5
		TPU670	TP-P5
		TPU671	TP-P5
		TPU672	TP-P5
59 58 56	USBC1 CC1	TPU673	TP-P5
59 58 56	USBC1 CC2	TPU674	TP-P5
59 58	USBC1 SBU1	TPU675	TP-P5
59 58	USBC1 SBU2	TPU676	TP-P5
	GND	TPU677	TP-P5
59	TP USBC0 PP20V	TPU678	TP-P5
59	TP USBC1 PP20V	TPU679	TP-P5

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74 73	AMR LEFT OR ND 1V8	TPU699	TP-P5

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101	PPBUS AON	TPU6A0	TP-P5
		TPU6A1	TP-P5
		TPU6A2	TP-P5
		TPU6A3	TP-P5
		TPU6A4	TP-P5
		TPU6A5	TP-P5
		TPU6A6	TP-P5
		TPU6A7	TP-P5
101	PP3V8 AON	TPU6A8	TP-P5
101	PPVDD_PCPU_AWAKE	TPU6A9	TP-P5
101	PPVDD_GPU_AWAKE	TPU6B0	TP-P5
101	PPVDD_CPU_SRAM_AWAKE	TPU6B1	TP-P5
101	PPVDD_ECPU_AWAKE	TPU6B2	TP-P5
102	PP1V8_AWAKE	TPU6B3	TP-P5
102	PP1V25_AWAKE_IO	TPU6B4	TP-P5
101	PPVDD_SOC_S1	TPU6B5	TP-P5
101	PPVDD_DISP_S1	TPU6B6	TP-P5
101	PPVDD_DCS_S1	TPU6B7	TP-P5
101	PP1V8_S2	TPU6B8	TP-P5
		TPU6F0	TP-P5
102	PP1V2_S2	TPU6B9	TP-P5
102	PP3V3_S2_UPC	TPU6C0	TP-P5
102	PP1V25_S2	TPU6C1	TP-P5
104 84	PP1V8_AON	TPU6C2	TP-P5
102	PP1V2_AWAKE_PLL	TPU6C3	TP-P5
101	PP0V88_S1	TPU6C4	TP-P5
103	PP0V805_S1_VDD_FIXED	TPU6C5	TP-P5
101	PP0V6_S1_VDDQL	TPU6C6	TP-P5
101	PP0V764_S1_SRAM	TPU6C7	TP-P5
103	PP1V2_S2_CIO	TPU6C8	TP-P5
101	PP1V06_S2_W_DRAM	TPU6C9	TP-P5
102	PP0V855_S2SW_CIO	TPU6D0	TP-P5
102	PP0V72_S2_VDD_LOW	TPU6D1	TP-P5
102	PP0V88_AWAKESW_NAND	TPU6D2	TP-P5
102	PP1V25_AWAKESW_VCCQ	TPU6D3	TP-P5
101	PP2V5_AWAKE_NAND	TPU6D4	TP-P5
104	PP3V3_S2SW_USB1	TPU6D5	TP-P5
104	PP3V3_S2SW_USB0	TPU6D6	TP-P5
104	PP3V3_AON	TPU6D7	TP-P5
104	PP3V3_S2	TPU6D8	TP-P5
104	PP5V_S2	TPU6D9	TP-P5
		TPU6E0	TP-P5
102	PP1V4_LDO_PREREG	TPU6E1	TP-P5
104 69 41	PP3V3_SW_LCD	TPU6E2	TP-P5
		TPU6E3	TP-P5
104	PP3V3_S2SW_SNS	TPU6E4	TP-P5
57 56 55	PP3V3_UPC0_LDO	TPU6E5	TP-P5
104	PPVOUT_LCDBKLT	TPU6E6	TP-P5
97 22	PPVBAT_AON_CHGR_REG	TPU6E7	TP-P5
		TPU6E8	TP-P5
		TPU6E9	TP-P5

DISPLAY

69	AUX_N	TPU6G0	TP-P5	
69	AUX_P	TPU6G1	TP-P5	
69	DP0_P	TPU6G2	TP-P5	GND_VOID=TRUE
69	DP0_N	TPU6G3	TP-P5	GND_VOID=TRUE
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69	DP1_N	TPU6G5	TP-P5	GND_VOID=TRUE
69	DP2_P	TPU6G6	TP-P5	GND_VOID=TRUE
69	DP2_N	TPU6G7	TP-P5	GND_VOID=TRUE
69	DP3_P	TPU6G8	TP-P5	GND_VOID=TRUE
69	DP3_N	TPU6G9	TP-P5	GND_VOID=TRUE
69 68	MIPI_FTCAM_DATA_ISOL_N	TPU6H0	TP-P5	
69 68	MIPI_FTCAM_DATA_ISOL_P	TPU6H1	TP-P5	
69 68	MIPI_FTCAM_CLK_ISOL_N	TPU6H2	TP-P5	GND_VOID=TRUE
69 68	MIPI_FTCAM_CLK_ISOL_P	TPU6H3	TP-P5	GND_VOID=TRUE
104 69	PP5V_SW_LCD	TPU6H4	TP-P5	
69 6	UART_TCON_HDMI_D2R	TPU6H5	TP-P5	
70 69	EDP_PANEL_1V8_EN	TPU6H6	TP-P5	
69 7	LPDP_INT_HPD	TPU6H7	TP-P5	
69 6	SPI_TCON_CS_L	TPU6H8	TP-P5	
69 6	SPI_TCON_MISO	TPU6H9	TP-P5	
69	SPI_TCON_MOSI	TPU6I0	TP-P5	
69	SPI_TCON_CLK	TPU6I1	TP-P5	
69 42	I2C_ALS_1V8_SDA	TPU6I2	TP-P5	
69 42	I2C_ALS_1V8_SCL	TPU6I3	TP-P5	
69 68	I2C_FTCAM_ISOL_SCL	TPU6I4	TP-P5	
69 68	I2C_FTCAM_ISOL_SDA	TPU6I5	TP-P5	
71 69	I2C_BKLT_SDA	TPU6I6	TP-P5	
71 69	I2C_BKLT_SCL	TPU6I7	TP-P5	
69 6	UART_TCON_HDMI_R2D	TPU6I8	TP-P5	
69 41	I2C_MLB2JERRY_3V3_SDA	TPU6I9	TP-P5	
69 41	I2C_MLB2JERRY_3V3_SCL	TPU6J0	TP-P5	
69	TP_TCON_SWCLK	TPU6J1	TP-P5	
69	TP_TCON_SWDIO	TPU6J2	TP-P5	
69	PP5V_CAM	TPU6J3	TP-P5	
	GND	TPU6J4	TP-P5	

AJ/MESA

80	AUD_CONN_LEFT_OUT	TPU6K0	TP-P5
80	AUD_CONN_SLEEVE	TPU6K1	TP-P5
80	AUD_CONN_RIGHT_OUT	TPU6K2	TP-P5
80	AUD_CONN_RING2	TPU6K3	TP-P5
80	AUD_CONN_TIP_SENSE	TPU6K4	TP-P5
80	AUD_CONN_LEFT_SNS	TPU6K5	TP-P5
80	AUD_CONN_RING2_XW	TPU6K6	TP-P5
80	AUD_CONN_RING_SENSE	TPU6K7	TP-P5
80	AUD_CONN_RIGHT_SNS	TPU6K8	TP-P5
	AUD_CONN_SLEEVE_XW	TPU6K9	TP-P5
86	PP1V8_TOUCHID_FILT_CONN	TPU6L0	TP-P5
86 80 6	SPI_TOUCHID_MISO	TPU6L1	TP-P5
80 18	SPI_TOUCHID_MOSI	TPU6L2	TP-P5
86 80	TOUCHID_INT_1V8_CONN	TPU6L3	TP-P5
80 18	SPI_TOUCHID_CLK	TPU6L4	TP-P5
86 80	TOUCHID_BOOST_EN	TPU6L5	TP-P5
104 73	PP1V8_AON	TPU6L6	TP-P5
86 80	PP16V0_TOUCHID_FILT_CONN	TPU6L7	TP-P5
0 74 73	AMR_RIGHT_OR_ND_1V8	TPU6L8	TP-P5
86	PP3V0_TOUCHID_FILT_CONN	TPU6L9	TP-P5
		TPU6M0	TP-P5
	GND	TPU6M1	TP-P5
76	GND_AUDIO_CODEC	TPU6M2	TP-P5

SPEAKER

79 77	SPKRAMP_A_OUTP	TPU6M3	TP-P5
		TPU6M4	TP-P5
		TPU6M5	TP-P5
79 77	SPKRAMP_A_OUTN	TPU6M6	TP-P5
		TPU6M7	TP-P5
		TPU6M8	TP-P5
79 77	SPKRAMP_B_OUTP	TPU6M9	TP-P5
		TPU6N0	TP-P5
		TPU6N1	TP-P5
79 77	SPKRAMP_B_OUTN	TPU6N2	TP-P5
		TPU6N3	TP-P5
		TPU6N4	TP-P5
7 6	SPKR_ID0	TPU6N5	TP-P5
	GND	TPU6N6	TP-P5
79 78	SPKRAMP_D_OUTP	TPU6N7	TP-P5
		TPU6N8	TP-P5
		TPU6N9	TP-P5
79 78	SPKRAMP_D_OUTN	TPU6P0	TP-P5
		TPU6P1	TP-P5
		TPU6P2	TP-P5
79 78	SPKRAMP_E_OUTP	TPU6P3	TP-P5
		TPU6P4	TP-P5
		TPU6P5	TP-P5
79 78	SPKRAMP_E_OUTN	TPU6P6	TP-P5
		TPU6P7	TP-P5
		TPU6P8	TP-P5
79 6	SPKR_ID1	TPU6P9	TP-P5
	GND	TPU6Q0	TP-P5

KEYBOARD

105	PP1V85_S2_KBD_ISNS	TPU6Q1	TP-P5
83 82	KBD_ID1	TPU6Q2	TP-P5
83 82	KBD_DRIVE_Y2	TPU6Q3	TP-P5
83 82	KBD_DRIVE_Y1	TPU6Q4	TP-P5
83 82	KBD_DRIVE_Y3	TPU6Q5	TP-P5
83 82	KBD_DRIVE_Y4	TPU6Q6	TP-P5
83 82	KBD_SENSE_X0	TPU6Q7	TP-P5
83 82	KBD_SENSE_X1	TPU6R0	TP-P5
83 82	KBD_SENSE_X2	TPU6R1	TP-P5
83 2	KBD_SENSE_X5	TPU6R2	TP-P5
83 82	KBD_SENSE_X3	TPU6R3	TP-P5
83 82	KBD_SENSE_X9	TPU6R4	TP-P5
83 82	KBD_SENSE_X12	TPU6R5	TP-P5
83 82	KBD_SENSE_X4	TPU6R6	TP-P5
83 82	KBD_SENSE_X11	TPU6R7	TP-P5
83 82	KBD_SENSE_X10	TPU6R8	TP-P5
83 82	KBD_SENSE_X6	TPU6R9	TP-P5
83 82	KBD_SENSE_X7	TPU6S0	TP-P5
83 82	KBD_SENSE_X8	TPU6S1	TP-P5
83 82	KBD_DRIVE_Y5	TPU6S2	TP-P5
83 82	KBD_DRIVE_Y7	TPU6S3	TP-P5
83 82	KBD_DRIVE_Y6	TPU6S4	TP-P5
83 82	KBD_DRIVE_Y0	TPU6S5	TP-P5
83 82	KBD_CAP_CATHODE	TPU6S6	TP-P5
83 82	PP3V3_AON_KBD_CONN	TPU6S7	TP-P5
83 82	KBD_RIGHT_SHIFT_KEY	TPU6S8	TP-P5
83 82	KBD_LEFT_OPTION_KEY	TPU6S9	TP-P5
83 82	KBD_CONTROL_KEY	TPU6T0	TP-P5
81	PPVOUT_S0_KBDLED_CONN	TPU6T1	TP-P5
	KBDLED_CATHODE1_R	TPU6T2	TP-P5
81 72	KBDLED_CATHODE1	TPU6T3	TP-P5
81 72	KBDLED_CATHODE2	TPU6T4	TP-P5
81	KBDLED_CATHODE2_R	TPU6T5	TP-P5
	GND	TPU6T6	TP-P5
72 71	GND_BKLT_SGND	TPU6T7	TP-P5
		TPU6T8	TP-P5
83 82	KBD_DRIVE_Y8	TPU6J5	TP-P5

DMIC

80 74	DMIC_CLK0_1V8_OUT	TPU6T9	TP-P5
80	AUD_DMIC0_DATA_CONN	TPU6U0	TP-P5
80	PP1V8_DMIC	TPU6U1	TP-P5
80 74	DMIC_CLK1_1V8_OUT	TPU6U2	TP-P5
80	AUD_DMIC1_DATA_CONN	TPU6U3	TP-P5
	GND	TPU6U4	TP-P5

TRACKPAD

87 85 73 33	IPD_LID_OPEN_1V8	TPU6U5	TP-P5
43	I2C_SMC_IPD_1V8_SCL	TPU6U6	TP-P5
85 34	TPAD_KBD_WAKE_L	TPU6U7	TP-P5
43	I2C_SMC_IPD_1V8_SDA	TPU6U8	TP-P5
85 82	KBD_INT_L	TPU6U9	TP-P5
85 4	SPI_TPAD_INT_CONN_L	TPU6V0	TP-P5
117 85 82	I2C_KBD_SDA	TPU6V1	TP-P5
85 84	SPI_TPAD_MOSI_CONN	TPU6V2	TP-P5
117 85 82	I2C_KBD_SCL	TPU6V3	TP-P5
85 84	SPI_TPAD_CS_CONN_L	TPU6V4	TP-P5
85 84	SPI_TPAD_MISO_CONN	TPU6V5	TP-P5
85 84	SPI_TPAD_EN_CONN	TPU6V6	TP-P5
85 84	SPI_TPAD_CLK_CONN	TPU6V7	TP-P5
85	PP5V_S2_TPAD_CONN	TPU6V8	TP-P5
		TPU6V9	TP-P5
104	PP1V85_S2_IPD	TPU6W0	TP-P5
105	PP3V3_S2_TPAD_ISNS	TPU6W1	TP-P5
		TPU6W2	TP-P5
		TPU6W3	TP-P5
85	ACT_GND	TPU6W4	TP-P5
		TPU6W5	TP-P5
		TPU6W6	TP-P5
		TPU6W7	TP-P5
	GND	TPU6W8	TP-P5

DFR

87	TP_DFR_TOUCH_PANEL_DETECT	TPU6W9	TP-P5
87	DFR_LID_OPEN_L	TPU6X0	TP-P5
87	DFR_DISP_VSYNC	TPU6X1	TP-P5
87	TP_DFR_TOUCH_RSVD	TPU6X2	TP-P5
88 87	SPI_1V8_DFR_MISO	TPU6X3	TP-P5
88 87	SPI_1V8_DFR_CS_L	TPU6X4	TP-P5
88 7	SPI_1V8_DFR_CLK	TPU6X5	TP-P5
88 87	SPI_1V8_DFR_MOSI	TPU6X6	TP-P5
88 87	DFR_1V8_TOUCH_INT_L	TPU6X7	TP-P5
41	I2C_DFR_RES_SCL	TPU6X8	TP-P5
88 87	DFR_1V8_TOUCH_CLK32K_RESET_L	TPU6X9	TP-P5
41	I2C_DFR_RES_SDA	TPU6Y0	TP-P5
88 87 6	DFR_1V8_TOUCH_RESET_L	TPU6Y1	TP-P5
87	TP_DFR_TOUCH_ROM_WC	TPU6Y2	TP-P5
88 87 41	PP1V8_AWAKE_DFR	TPU6Y3	TP-P5
		TPU6Y4	TP-P5
		TPU6Y5	TP-P5
		TPU6Y6	TP-P5
87	PP5V_S2_DFR_FILT	TPU6Y7	TP-P5
	GND	TPU6Y8	TP-P5
87	MIPI_DFR_CLK_CONN_FILT_P	TPU6Y9	TP-P5
87	MIPI_DFR_CLK_CONN_FILT_N	TPU6Z0	TP-P5
88 87	DFR_1V8_DISP_TE	TPU6Z1	TP-P5
87	MIPI_DFR_DATA_CONN_FILT_P	TPU6Z2	TP-P5
88 87 6	DFR_1V8_DISP_INT	TPU6Z3	TP-P5
8	MIPI_DFR_DATA_CONN_FILT_N	TPU6Z4	TP-P5
88 87 6	DFR_1V8_DISP_RESET_L	TPU6Z5	TP-P5
87	PP3V3_AWAKE_DFR	TPU6Z6	TP-P5
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		TPU6Z8	TP-P5
	GND	TPU6Z9	TP-P5

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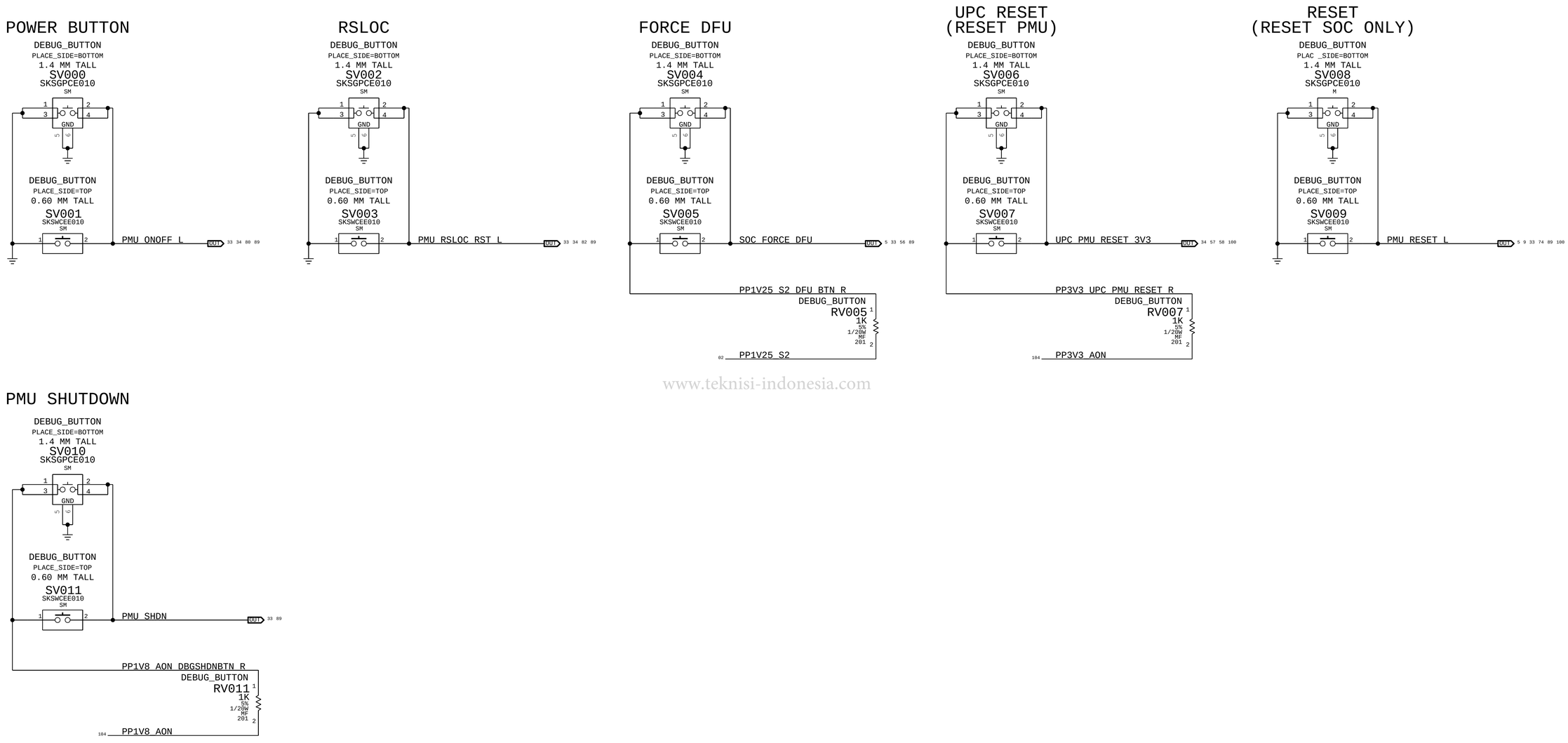

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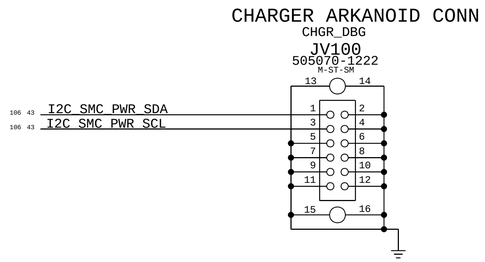

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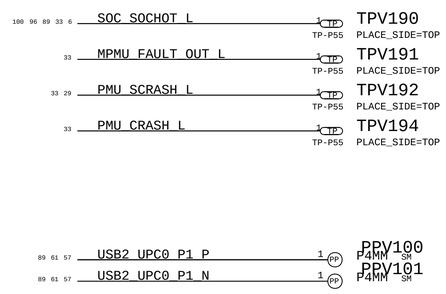

SYNC_MASTER=T668_MLB SYNC_DATE=06/20/2019

PAGE TITLE

DEBUG: MISC

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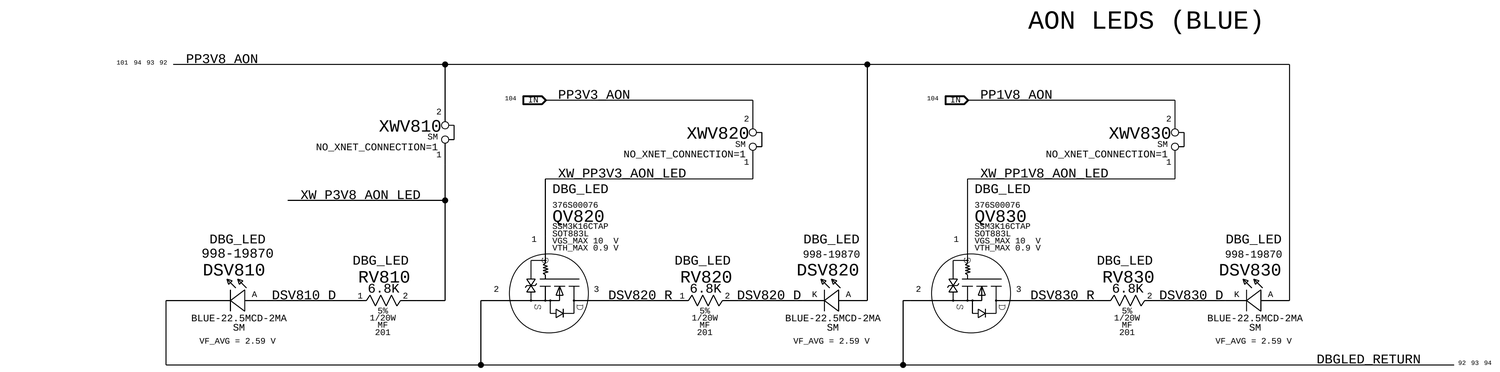

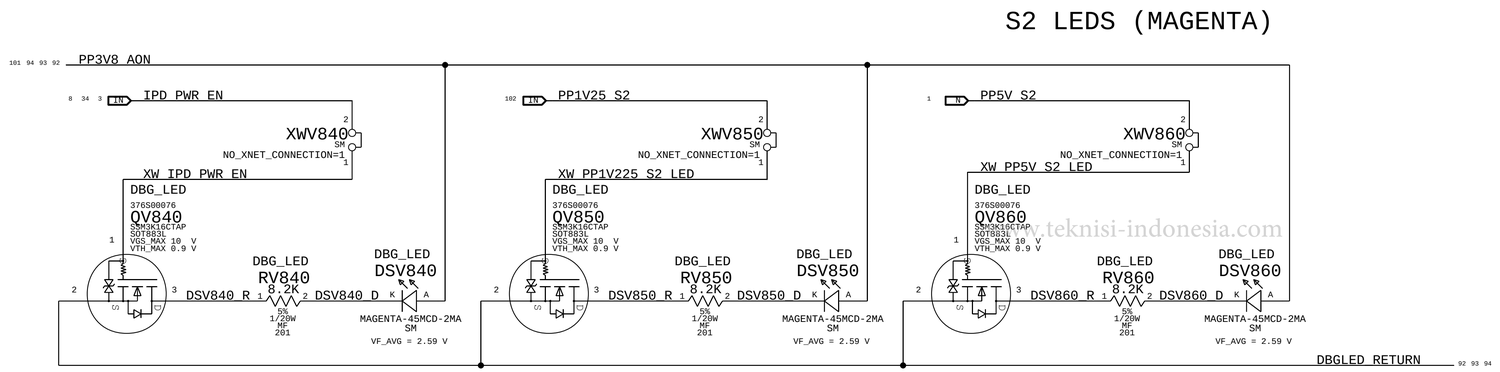

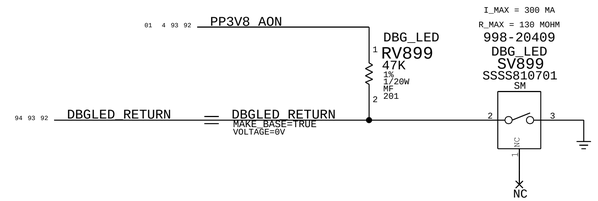

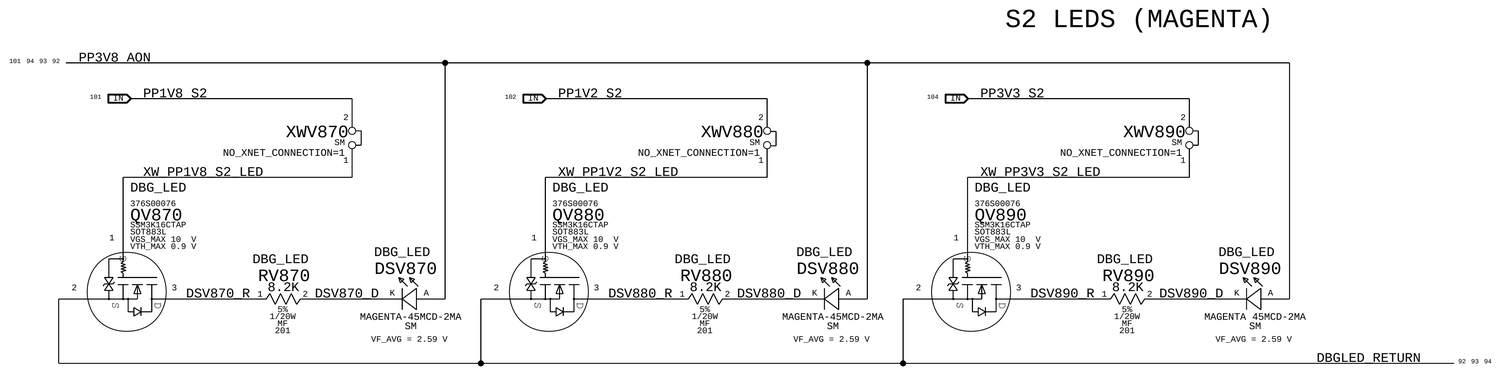

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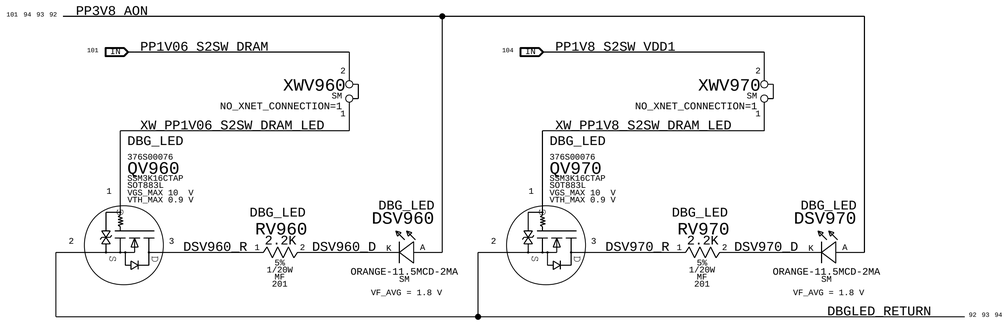
BOM_COST_GROUP=DEBUG

SYNC_MASTER=T668_MLB SYNC_DATE=07/24/2019

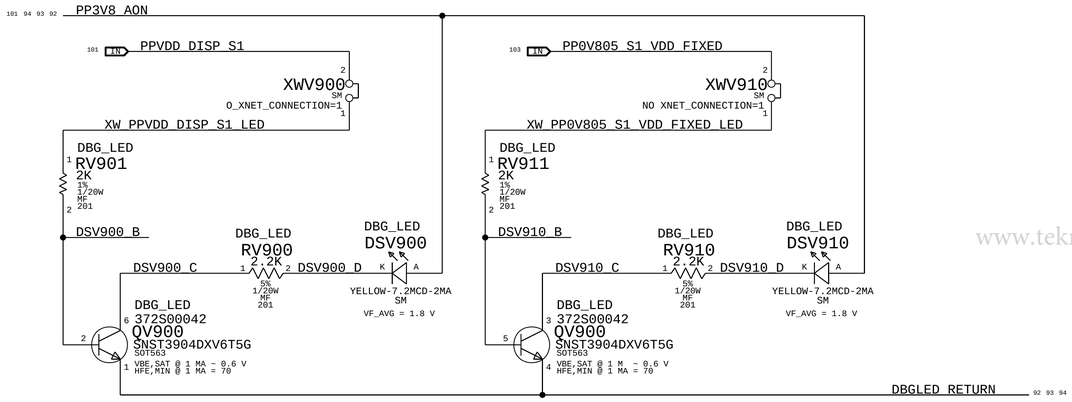
PAGE TITLE

DEBUG: LEDS (1/3)

S2SW LEDS (ORANGE)



S1 LEDS (YELLOW)



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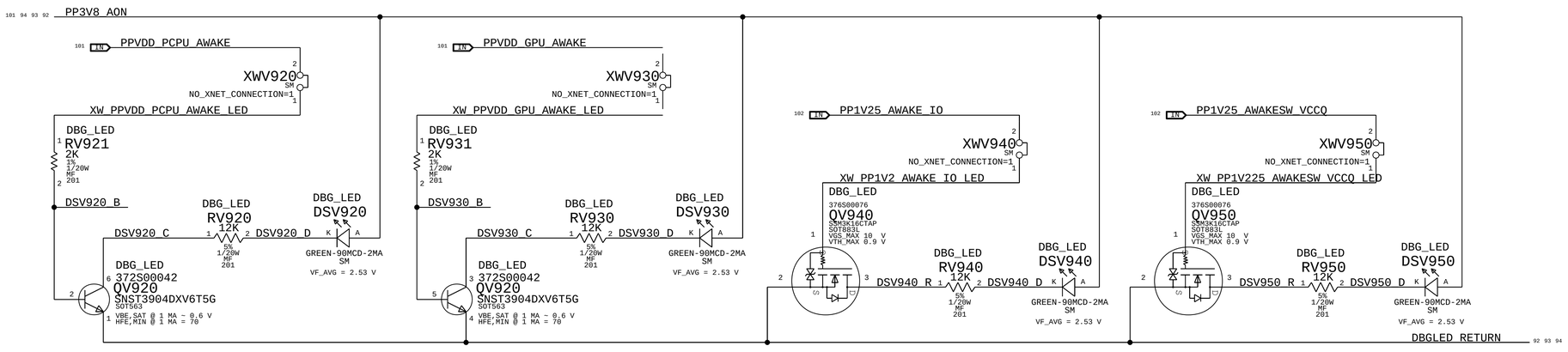
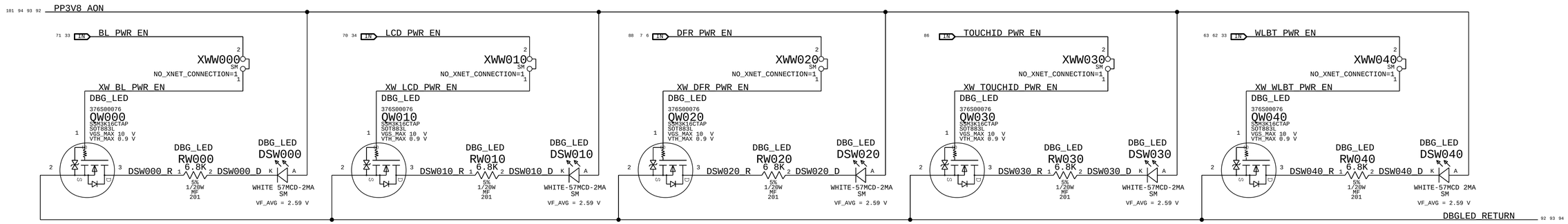
AWAKE LEDS (GREEN)



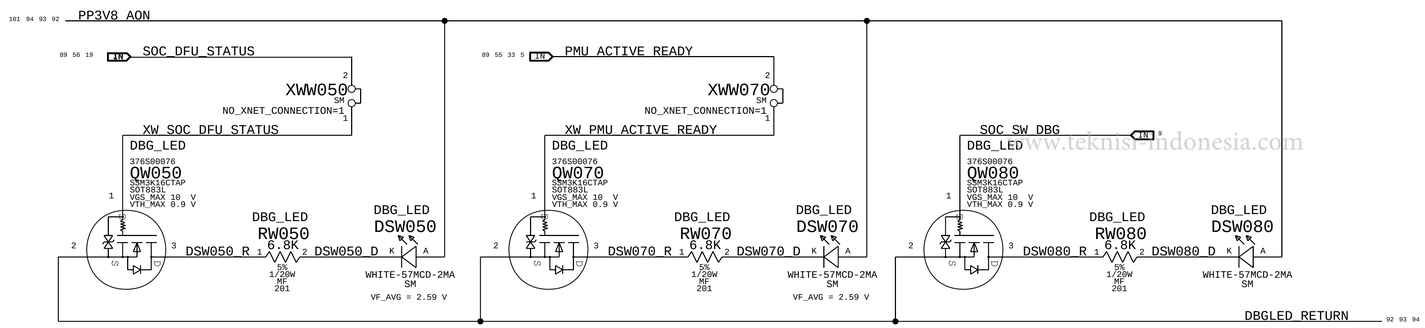
BOM_COST_GROUP=DEBUG

SYNC_MASTER=T668_MLB	SYNC_DATE=07/24/2019
PAGE TITLE	
DEBUG: LEDS (2/3)	

MODULE LEDS (WHITE)



STATUS LEDS (WHITE)



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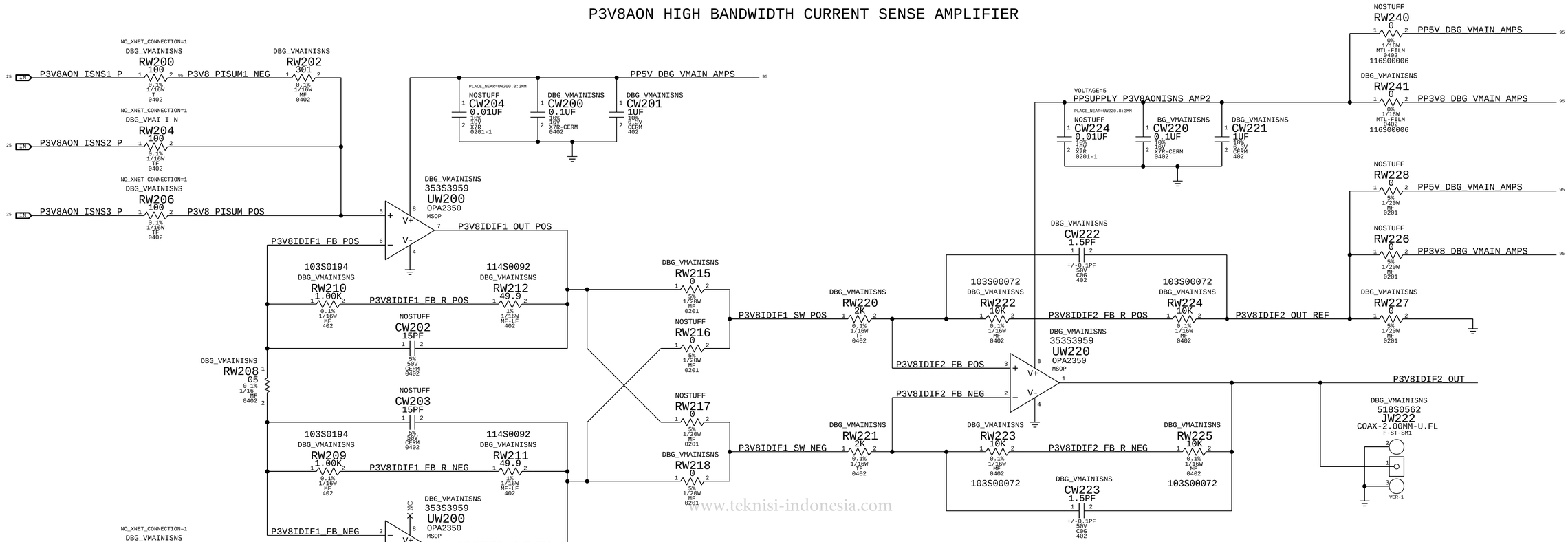
BOM_COST_GROUP=DEBUG

SYNC_MASTER=T668_MLB SYNC_DATE=07/24/2019

PAGE TITLE

DEBUG: LEDS (3/3)

P3V8AON HIGH BANDWIDTH CURRENT SENSE AMPLIFIER



STUFF THESE TO ENABLE VMAIN SENSE AMP

NOTE: IF THESE ARE STUFFED, THEN THERE WILL BE SOME LEAKAGE IN OFF ONTO 5V_S2 THROUGH UW200 <RDAR://57211269>

CHAD NOTES:
EFFECTIVE CURRENT SENSE R = 0.4444 MOHM
1 MOHM || 1 MOHM || 4 MOHM
STAGE 1 GAIN = 11.243
STAGE 1 BANDWIDTH ~ 3.38 MHZ
STAGE 1 OUTPUT SCALE = 5.00 MV/A
STAGE 2 GAIN = 10.00
STAGE 2 BANDWIDTH ~ 3.80 MHZ
STAGE 2 OUTPUT SCALE = 50.0 MV/A

SYNC_MASTER=T668_MLB SYNC_DATE=06/20/2019

PAGE TITLE

DEBUG: P3V8AON ISENSE

BOM_COST_GROUP=DEBUG

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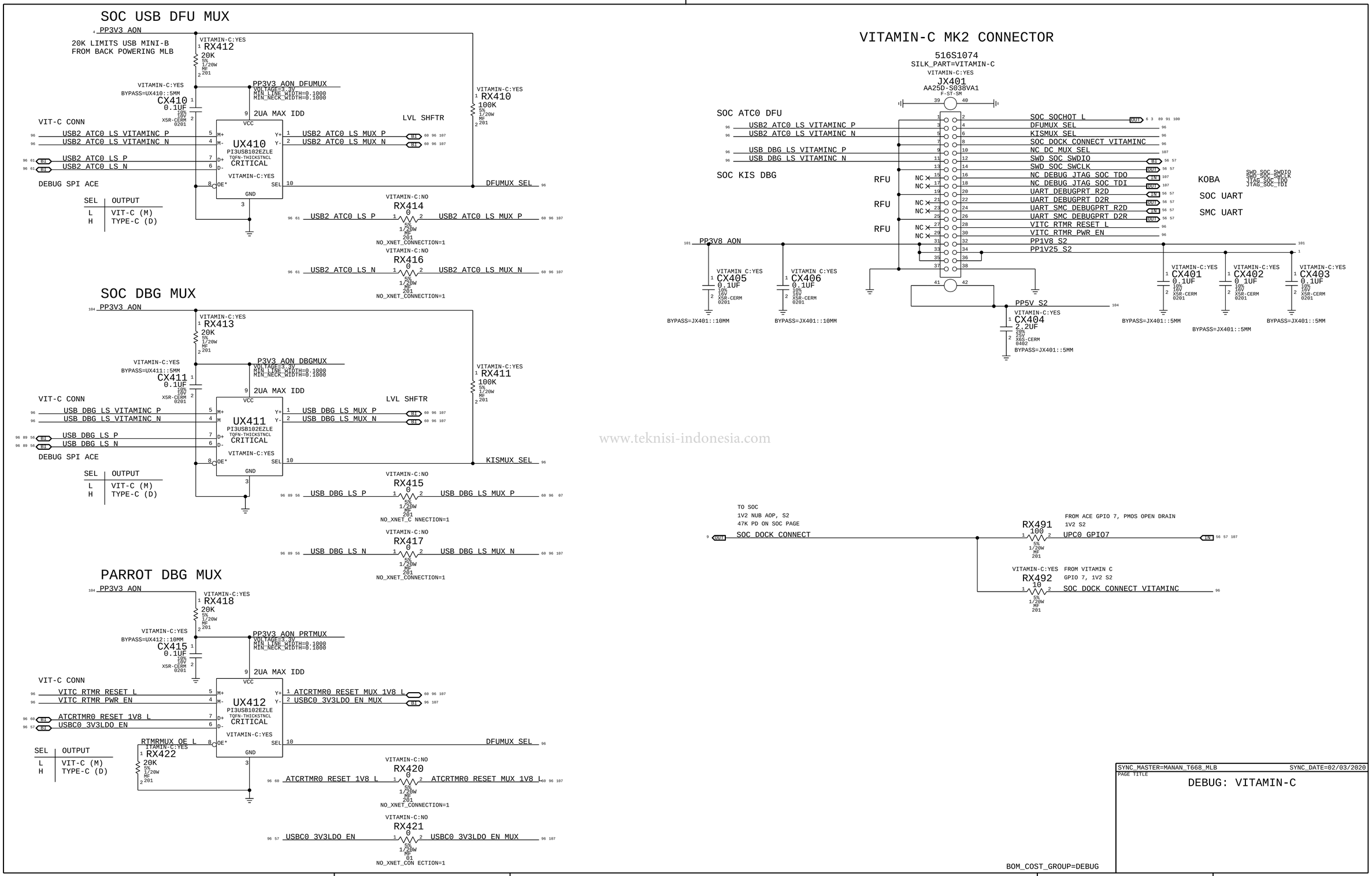

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SYNC_MASTER=KEI_T668_MLB SYNC_DATE=11/04/2010

PAGE TITLE

DESENSE (1/3)

P3V8AON VIN

105 PPBUS_VMAIN_VIN_ISNS

CY110 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY111 1 12PF 5% 25V NP0-C0G 0201 2
CY112 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY113 1 12PF 5% 25V NP0-C0G 0201 2
CY114 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY115 1 12PF 5% 25V NP0-C0G 0201 2

CY116 1 12PF 5% 25V NP0-C0G 0201 2
CY117 1 12PF 5% 25V NP0-C0G 0201 2
CY118 1 12PF 5% 25V NP0-C0G 0201 2
CY1C0 1 12PF 5% 25V NP0-C0G 0201 2
CY1C1 1 12PF 5% 25V NP0-C0G 0201 2
CY1C2 1 12PF 5% 25V NP0-C0G 0201 2
CY1C3 1 12PF 5% 25V NP0-C0G 0201 2

P3V8AON

101 PP3V8_AON

CY120 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY121 1 12PF 5% 25V NP0-C0G 0201 2
CY122 1 3.0PF +/-0.1PF NP0-C0G 2
CY123 1 12PF 5% 25V NP0-C0G 0201 2
CY124 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY125 1 12PF 5% 25V NP0-C0G 0201 2
CY12A 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY12B 1 12PF 5% 25V NP0-C0G 0201 2

CY126 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY127 1 12PF 5% 25V NP0-C0G 0201 2
CY128 1 3.0PF +/-0.1PF 2.V NP -C0 0201 2
CY129 1 12PF 5% 25V NP0-C0G 0201 2
CY12C 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY12D 1 12PF 5% 2.V NP0 C0G 0201 2

5V S2

104 PP5V_S2

CY130 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY131 1 12PF 5% 25V NP0-C0G 0201 2

5V S2 VIN

105 PPBUS_AON_5VS2_VIN_ISNS

CY140 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY141 1 12PF 5% 25V NP0-C0G 0201 2
CY142 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY143 1 12PF 5% 25V NP0-C0G 0201 2

KBD BACKLIGHT

104 PPVOUT_KBDLED

CY150 1 3PF +/-0.1PF 100V C0G 0201 2 131S00140
CY151 1 12PF 5% 100V CERM 0402 2 131S00041

PBUS

101 PPBUS_AON

CY160 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY161 1 12PF 5% 25V NP0-C0G 0201 2
CY162 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY163 1 12PF 5% 25V NP0-C0G 0201 2

BUCK 13

102 7 PP1V25_S2

CY170 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY171 1 12PF 5% 25V NP0-C0G 0201 2
CY172 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY173 1 12PF 5% 25V NP0-C0G 0201 2
CY174 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY175 1 12PF 5% 25V NP0-C0G 0201 2

CY176 1 3.0PF +/-0.1PF 25V NP0-C0 0201 2
CY177 1 12PF 5% 25V NP0-C0G 0201 2

1V8 AON

104 PP1V8_AON

CY180 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY181 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY182 1 12PF 5% 25V NP0-C0G 0201 2
CY183 1 12PF 5% 25V NP0-C0G 0201 2

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DCIN

89 22 PPDCIN_AON_CHGR_R

CY190 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2
CY191 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2

LCD BACKLIGHT

104 PPVOUT_LCDBKLT

CY1A0 1 3PF +/-0.1PF 100V C0G 0201 2 131S00140
CY1A1 1 12PF 5% 100V CERM 0402 2 131S00041

DCIN

101 PPDCIN_USBC_AON

CY1B0 1 3.0PF +/-0.1PF 25V NP0 C0G 0201 2
CY1B1 1 3.0PF +/-0.1PF 25V NP0-C0G 0201 2

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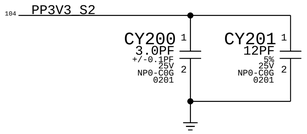
SYNC_MASTER=KEI_T668_MLB SYNC_DATE=09/30/2019

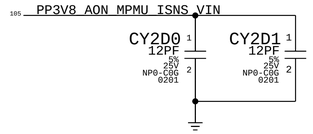
PAGE TITLE

DESENSE (2/3)

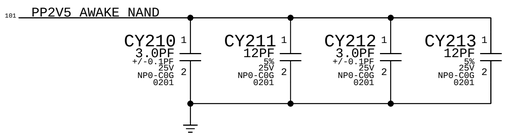
3V3 S2

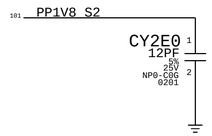


MASTER PMU HIGH SIDE INPUT

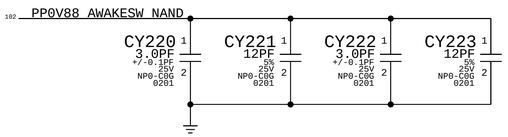


2V5 AWAKE NAND

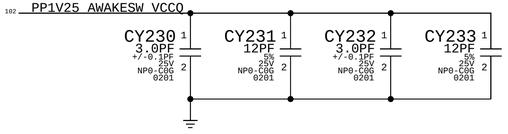




0V88 AWAKESW NAND



1V25 AWAKESW VCCQ



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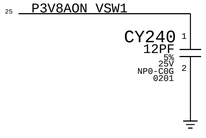
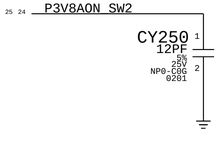
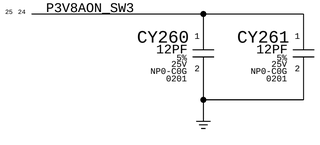
VMAIN SWITH NODE PHASE 1



VMAIN SWITH NODE PHASE 2



VMAIN SWITH NODE PHASE 3



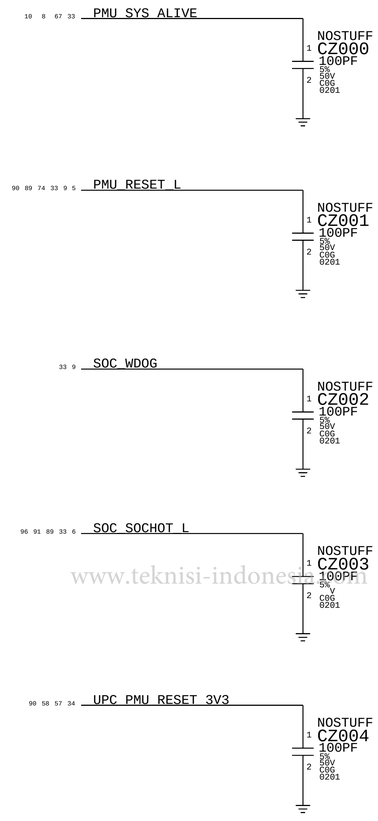
BOM_COST_GROUP=DESENSE

SYNC_MASTER=KEI_T668_MLB SYNC_DATE=09/30/2019

PAGE TITLE

DESENSE (3/3)

EMC REQUESTS FOR CAPS ON SOME SIGNALS
NO-STUFF'ED UNTIL WE GET CONFIRMATION / DATA IF THEY ARE NEEDED
<RDAR://58576418>



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SYNC_MASTER=KEI_T668_MLB SYNC_DATE=10/02/2019

PAGE TITLE

EMC

BOM_COST_GROUP=EMC

VBAT

21 PPVBAT_AON

- PPVBAT_AON — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1500, MIN_LINE_WIDTH=0.6000, VOLTAGE=13.05V — 89
- PPVBAT_AON — 22

USBC DCIN

55 PPDCIN_USBC_AON

- PPDCIN_USBC_AON — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=13.1 — 89
- PPDCIN_USBC_AON — 22
- PPDCIN_USBC_AON — 44 48
- PPDCIN_USBC_AON — 98

PBUS

22 PPBUS_AON

- PPBUS_AON — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=13.1 — 89
- PPBUS_AON — 44
- PPBUS_AON — 46
- PPBUS_AON — 46
- PPBUS_AON — 1
- PP_US_AON
- PPBUS_AON — 31
- PPBUS_AON — 44
- PPBUS_AON — 44
- PPBUS_AON — 44
- PPBUS_AON — 98

ICEMAN VMAIN

25 PP3V8_AON

- PP3V8_AON — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=3.8 — 89
- PP3V8_AON — 45
- PP3V8_AON — 45
- PP3V8_AON — 84
- PP3V8_AON — 76
- PP3V8_AON — 21
- PP3V8_AON
- PP3V8_AON — 45
- PP3V8_AON — 35
- PP3V8_AON — 45
- PP3V8_AON — 92 93 94
- PP3V8_AON — 84
- PP3V8_AON — 35
- PP3V8_AON — 20
- PP3V8_AON — 95
- PP3V8_AON — 39
- PP3V8_AON — 6
- PP3V8_AON — 98

ICEMAN LDO5

24 PP5V_AON

- PP5V_AON — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=5.1
- PP5V_AON — 24

MPMU BUCK 0

31 PPVDD_PCPU_AWAKE

- PPVDD_PCPU_AWAKE — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=1.06 — 89
- PPVDD_PCPU_AWAKE — 12
- PPVDD_PCPU_AWAKE — 93
- PPVDD_PCPU_AWAKE — 97

MPMU BUCK 1

34 31 PPVDD_GPU_AWAKE

- PPVDD_GPU_AWAKE — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=1.06 — 89
- PPVDD_GPU_AWAKE — 12
- PPVDD_GPU_AWAKE — 93
- PPVDD_GPU_AWAKE — 97

MPMU BUCK 2

31 PPVDD_SOC_S1

- PPVDD_SOC_S1 — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=0.857 — 89
- PPVDD_SOC_S1 — 12
- PPVDD_SOC_S1 — 97

MPMU BUCK 3

32 PP1V8_S2

- PP1V8_S2 — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=1.8 — 89
- PP1V8_S2 — 39
- PP1V8_S2 — 31
- PP1V8_S2 — 27
- PP1V8_S2 — 22 23
- PP1V8_S2 — 52
- PP1V8_S2 — 32
- PP1V8_S2 — 28
- PP1V8_S2 — 56 57 60
- PP1V8_S2 — 56 60
- PP1V8_S2 — 46
- PP1V8_S2 — 92
- PP1V8_S2 — 56 58 60
- PP1V8_S2 — 46
- PP1V8_S2 — 42
- PP1V8_S2 — 74
- PP1V8_S2 — 43
- PP1V8_S2 — 43
- PP1V8_S2 — 51
- PP1V8_S2 — 70
- PP1V8_S2 — 20
- PP1V8_S2 — 68
- PP1V8_S2 — 80
- PP1V8_S2 — 42
- PP1V8_S2 — 84
- PP1V8_S2 — 96
- PP1V8_S2 — 99

SPMU BUCK 4

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27 PP1V06_S2SW_DRAM

- PP1V06_S2SW_DRAM — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=1.06 — 89
- PP1V06_S2SW_DRAM — 10
- PP1V06_S2SW_DRAM — 28
- PP1V06_S2SW_DRAM — 97
- PP1V06_S2SW_DRAM — 93

SPMU BUCK 5

27 PP0V764_S1_SRAM

- PP0V764_S1_SRAM — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=0.764 — 89
- PP0V764_S1_SRAM — 13 48
- PP0V764_S1_SRAM — 97

SPMU BUCK 6

27 PP2V5_AWAKE_NAND

- PP2V5_AWAKE_NAND — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=2.5 — 89
- PP2V5_AWAKE_NAND — 64 65 66
- PP2V5_AWAKE_NAND — 99

MPMU BUCK 7

32 PPVDD_CPU_SRAM_AWAKE

- PPVDD_CPU_SRAM_AWAKE — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=1.06 — 89
- PPVDD_CPU_SRAM_AWAKE — 13 48
- PPVDD_CPU_SRAM_AWAKE — 97

MPMU BUCK 8

PPVDD_DISP_S1

- PPVDD_DISP_S1 — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=0.942 — 89
- PPVDD_DISP_S1 — 2
- PPVDD_DISP_S1 — 3
- PPVDD_DISP_S1 — 97

MPMU BUCK 9

PPVDD_DCS_S1

- PPVDD_DCS_S1 — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=0.842 — 89
- PPVDD_DCS_S1 — 3
- PPVDD_DCS_S1 — 97

SPMU BUCK 10

27 PP0V6_S1_VDDQL

- PP0V6_S1_VDDQL — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=0.6 — 89
- PP0V6_S1_VDDQL — 10
- PP0V6_S1_VDDQL — 97

MPMU BUCK 11

32 PPVDD_ECPU_AWAKE

- PPVDD_ECPU_AWAKE — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=1.06 — 9
- PPVDD_ECPU_AWAKE — 12
- PPVDD_ECPU_AWAKE — 97

SPMU BUCK 12

27 PP0V88_S1

- PP0V88_S1 — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, VOLTAGE=0.88 — 89
- PP0V88_S1 — 28
- PP0V88_S1 — 97

SYNC_MASTER=M42_T666_MLB — SYNC_DATE=11/06/2023

PAGE TITLE

POWER ALIASES 1

SPMU BUCK 13

```
27 PP1V25_S2                    PP1V25_S2
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=1.25
                                89
                                PP1V25_S2                    11
                                PP1V25_S2                    11
                                PP1V25_S2                    14
                                PP1V25_S2                    14
                                PP1V25_S2                    28 29
                                PP1V25_S2                    32
                                PP1V25_S2                    23
                                PP1V25_S2                    27
                                PP1V25_S2                    31
                                PP1V25_S2                    3
                                PP1V25_S2                    2
                                PP1V25_S2                    52
                                PP1V25_S2                    55 57 58
                                PP1V25_S2                    34
                                PP1V25_S2                    28
                                PP1V25_S2                    92
                                PP1V25_S2                    60
                                PP1V25_S2                    14
                                PP1V25_S2                    33
                                PP1V25_S2                    2
                                PP1V25_S2                    3
                                PP1V25_S2                    43
                                PP1V25_S2                    51
                                PP1V25_S2                    41
                                PP1V25_S2                    42
                                PP1V25_S2                    43
                                PP1V25_S2                    43
                                PP1V25_S2                    86
                                PP1V25_S2                    62
                                PP1V25_S2                    76
                                PP1V25_S2                    20
                                PP1V25_S2                    96
                                PP1V25_S2                    90
                                PP1V25_S2                    84
                                PP1V25_S2                    97 98
                                PP1V25_S2                    41
```

MPMU BUCK 14

```
34 PP1V4_LDO_PREREG             PP1V4_LDO_PREREG
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=1.4
                                89
                                PP1V4_LDO_PREREG             34
```

MPMU BUCK 3 SW 1

```
32 PP1V8_AWAKE                  PP1V8_AWAKE
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=1.8
                                89
                                PP1V8_AWAKE                  11 97
                                PP1V8_AWAKE                  4
                                PP1V8_AWAKE                  7
                                PP1V8_AWAKE                  17
                                PP1V8_AWAKE                  4
                                PP1V8_AWAKE                  76
                                PP1V8_AWAKE                  75 77 78
                                PP1V8_AWAKE                  41
                                PP1V8_AWAKE                  41
```

MPMU BUCK 3 SW 2

(NOT USED)

MPMU BUCK 13 SW 3

```
32 PP1V25_AWAKE_IO              PP1V25_AWAKE_IO
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=1.225
                                89
                                PP1V25_AWAKE_IO              4 5 6 8 11
                                PP1V25_AWAKE_IO              14
                                PP1V25_AWAKE_IO              14
                                PP1V25_AWAKE_IO              14
                                PP1V25_AWAKE_IO              14
                                PP1V25_AWAKE_IO              14
                                PP1V25_AWAKE_IO              14
                                PP1V25_AWAKE_IO              88
                                PP1V25_AWAKE_IO              79
                                PP1V25_AWAKE_IO              93
                                PP1V25_AWAKE_IO              84
                                PP1V25_AWAKE_IO              17
                                PP1V25_AWAKE_IO              4
                                PP1V25_AWAKE_IO              75 76 77
                                PP1V25_AWAKE_IO              34
                                PP1V25_AWAKE_IO              76
                                PP1V25_AWAKE_IO              41
                                PP1V25_AWAKE_IO              41
                                PP1V25_AWAKE_IO              41
                                PP1V25_AWAKE_IO              41
```

SPMU BUCK 3 SW 4

(NOT USED EXTERNALLY, SPMU GPIOS ONLY)

SPMU BUCK 13 SW 5

```
28 PP1V25_AWAKESW_VCCQ          PP1V25_AWAKESW_VCCQ
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=1.225
                                89
                                PP1V25_AWAKESW_VCCQ          64 65
                                PP1V25_AWAKESW_VCCQ          93
                                PP1V25_AWAKESW_VCCQ          99
```

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SPMU BUCK 12 SW 6

```
28 PP0V88_AWAKESW_NAND          PP0V88_AWAKESW_NAND
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=0.88
                                89
                                PP0V88_AWAKESW_NAND          64
                                PP0V88_AWAKESW_NAND          65
                                PP0V88_AWAKESW_NAND          99
```

SPMU BUCK 12 SW 7

TIED TO SW6

MPMU LDO 1

```
33 NC_MPMU_VLDO1                NC_MPMU_VLDO1
                                MAKE_BASE=TRUE          NO_TEST=1
```

MPMU LDO 2

(NOT USED)

MPMU LDO 3

```
33 PP1V2_S2                     PP1V2_S2
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=1.225
                                89
                                PP1V2_S2                     74
                                PP1V2_S2                     92
```

SPMU LDO 4

```
28 PP0V72_S2_VDD_LOW            PP0V72_S2_VDD_LOW
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=0.72
                                89
                                PP0V72_S2_VDD_LOW            14
                                PP0V72_S2_VDD_LOW            14
                                PP0V72_S2_VDD_LOW            14
                                PP0V72_S2_VDD_LOW            14 48
                                PP0V72_S2_VDD_LOW            14
```

MPMU LDO 5

```
33 NC_MPMU_VLDO5                NC_MPMU_VLDO5
                                MAKE_BASE=TRUE          NO_TEST=1
```

SPMU LDO 6

```
28 NC_SPMU_VLDO6                NC_SPMU_VLDO6
                                MAKE_BASE=TRUE          NO_TEST=1
```

MPMU LDO 7

```
33 PP3V3_S2_UPC                 PP3V3_S2_UPC
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=3.3V
                                89
                                PP3V3_S2_UPC                 55 57 58
```

SPMU LDO 8

```
28 PP1V2_AWAKE_PLL              PP1V2_AWAKE_PLL
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=1.2
                                89
                                PP1V2_AWAKE_PLL              10
                                PP1V2_AWAKE_PLL              14
                                PP1V2_AWAKE_PLL              14
                                PP1V2_AWAKE_PLL              14
```

MPMU LDO 9

NOT TO BE USED TO SOURCE POWER TO OTHER DEVICES

```
33 PP1V8_AON_MPMU               PP1V8_AON_MPMU
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=1.8V
                                PP1V8_AON_MPMU               29 33 34 35
```

SPMU LDO 9

NOT TO BE USED TO SOURCE POWER TO OTHER DEVICES

```
28 PP1V8_AON_SPMU               PP1V8_AON_SPMU
                                MAKE_BASE=TRUE
                                VOLTAGE=1.8
```

MPMU LDO 10

```
33 NC_MPMU_VLDO10               NC_MPMU_VLDO10
                                MAKE_BASE=TRUE          NO_TEST=1
```

SPMU LDO 11

```
28 PP0V855_S2SW_CIO             PP0V855_S2SW_CIO
                                MAKE_BASE=TRUE
                                MIN_NECK_WIDTH=0.1000
                                MIN_LINE_WIDTH=0.2000
                                VOLTAGE=0.855
                                89
                                PP0V855_S2SW_CIO             14
                                PP0V855_S2SW_CIO             14
```

SYNC_MASTER=KEI_T668_MLB SYNC_DATE=11/06/2010

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A

4 | 2 | 1

SPMU LDO12

28 PP0V805_S1_VDD_FIXED

PP0V805_S1_VDD_FIXED
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=0.805
89

PP0V805_S1_VDD_FIXED 1
PP0V805_S1_VDD_FIXED 14
PP0V805_S1_VDD_FIXED 14
PP0V805_S1_VDD_FIXED 14
PP0V805_S1_VDD_FIXED 14
PP0V805_S1_VDD_FIXED 14
PP0V805_S1_VDD_FIXED 14
PP0V805_S1_VDD_FIXED 14
PP0V805_S1_VDD_FIXED 14 97
PP0V805_S1_VDD_FIXED 93

SPMU LDO18

28 NC_SPMU_VLDO18

NC_SPMU_VLDO18
MAKE_BASE=TRUE NO_TEST=1

MPMU LDO19

(NOT USED)

SPMU LDO20

28 PP1V2_S2_CIO

PP1V2_S2_CIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.2
89

PP1V2_S2_CIO 14
PP1V2_S2_CIO 1
PP1V2_S2_CIO 97

MPMU LDO13

33 NC_MPMU_VLDO13

NC_MPMU_VLDO13
MAKE_BASE=TRUE NO_TEST=1

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MPMU LDO14

3 NC_MPMU_VLDO14

NC_MPMU_VLDO14
MAKE_BASE=TRUE NO_TEST=1

SPMU LDO15

28 NC_SPMU_VLDO15

NC_SPMU_VLDO15
MAKE_BASE=TRUE NO_TEST=1

MPMU LDO16

33 NC_MPMU_VLDO16

NC_MPMU_VLDO16
MAKE_BASE=TRUE NO_TEST=1

SPMU LDO17

28 NC_SPMU_VLDO17

NC_SPMU_VLDO17
MAKE_BASE=TRUE NO_TEST=1

SYNC_MASTER=T668_MLB SYNC_DATE=06/05/2019

PAGE TITLE

POWER ALIASES 3

KEYBOARD BACKLIGHT

```
72 PPVOUT_KBDLED ═══ PPVOUT_KBDLED
                     MAKE_BASE=TRUE
                     MIN_NECK_WIDTH=0.1000
                     MIN_LINE_WIDTH=0.2000
                     VOLTAGE=40
                     ═══ PPVOUT_KBDLED   81
                     ═══ PPVOUT_KBDLED   98
```

DISPLAY BACKLIGHT

```
71 PPVOUT_LCDBKLT ═══ PPVOUT_LCDBKLT
                      MAKE_BASE=TRUE
                      MIN_NECK_WIDTH=0.1000
                      MIN_LINE_WIDTH=0.2000
                      VOLTAGE=47
                      ═══ PPVOUT_LCDBKLT   69
                      ═══ PPVOUT_LCDBKLT   98
```

3V3 S2 VR

```
38 PP3V3_S2 ═══ PP3V3_S2
                MAKE_BASE=TRUE
                MIN_NECK_WIDTH=0.1000
                MIN_LINE_WIDTH=0.2000
                VOLTAGE=3.3
                ═══ PP3V3_S2   46
                ═══ PP3V3_S2   72
                ═══ PP3V3_S2   68
                ═══ PP3V3_S2   39
                ═══ PP3V3_S2   92
                ═══ PP3V3_S2   70
                ═══ PP3V3_S2   38
                ═══ PP3V3_S2   82
                ═══ PP3V3_S2   99
                ═══ PP3V3_S2   43
                ═══ PP3V3_S2   52
```

3V3 AON LDO (NEEDS REVIEW)

```
35 PP3V3_AON ═══ PP3V3_AON
                 MAKE_BASE=TRUE
                 MIN_NECK_WIDTH=0.1000
                 MIN_LINE_WIDTH=0.2000
                 VOLTAGE=3.3
                 ═══ PP3V3_AON   82
                 ═══ PP3V3_AON   92
                 ═══ PP3V3_AON   43
                 ═══ PP3V3_AON   34
                 ═══ PP3V3_AON   90
                 ═══ PP3V3_AON   96
                 ═══ PP3V3_AON   96
                 ═══ PP3V3_AON   96
```

3V3 SENSOR SWITCH

```
39 PP3V3_S2SW_SNS ═══ PP3V3_S2SW_SNS
                      MAKE_BASE=TRUE
                      MIN_NECK_WIDTH=0.1000
                      MIN_LINE_WIDTH=0.2000
                      VOLTAGE=3.3
                      ═══ PP3V3_S2SW_SNS   44 45 46 47
                      ═══ PP3V3_S2SW_SNS   43 50
                      ═══ PP3V3_S2SW_SNS   48
```

5V S2

```
36 PP5V_S2 ═══ PP5V_S2
               MAKE_BASE=TRUE
               MIN_NECK_WIDTH=0.1000
               MIN_LINE_WIDTH=0.2000
               VOLTAGE=5
               ═══ PP5V_S2   70
               ═══ PP5V_S2   52
               ═══ PP5V_S2   46
               ═══ PP5V_S2   57 58
               ═══ PP5V_S2   57 58
               ═══ PP5V_S2   71
               ═══ PP5V_S2   26
               ═══ PP5V_S2    7
               ═══ PP5V_S2   47
               ═══ PP5V_S2   92
               ═══ PP5V_S2   95
               ═══ PP5V_S2   87
               ═══ PP5V_S2   36
               ═══ PP5V_S2   96
               ═══ PP5V_S2   98
```

1V85 IPD

```
84 PP1V85_S2_IPD ═══ PP1V85_S2_IPD   89
                     MAKE_BASE=TRUE
                     MIN_NECK_WIDTH=0.1000
                     MIN_LINE_WIDTH=0.2000
                     VOLTAGE=1.85
                     ═══ PP1V85_S2_IPD   46
                     ═══ PP1V85_S2_IPD   47
```

USB0 3V3

```
53 PP3V3_S2SW_USB0 ═══ PP3V3_S2SW_USB0   89
                       MAKE_BASE=TRUE
                       MIN_NECK_WIDTH=0.1000
                       MIN_LINE_WIDTH=0.2000
                       VOLTAGE=3.3
                       ═══ PP3V3_S2SW_USB0   53 55
                       ═══ PP3V3_S2SW_USB0   53 55
                       ═══ PP3V3_S2SW_USB0   60
                       ═══ PP3V3_S2SW_USB0   60
```

USB1 3V3

```
54 PP3V3_S2SW_USB1 ═══ PP3V3_S2SW_USB1   89
                       MAKE_BASE=TRUE
                       MIN_NECK_WIDTH=0.1000
                       MIN_LINE_WIDTH=0.2000
                       VOLTAGE=3.3
                       ═══ PP3V3_S2SW_USB1   54
                       ═══ PP3V3_S2SW_USB1   54 55
                       ═══ PP3V3_S2SW_USB1   46
                       ═══ PP3V3_S2SW_USB1   60
```

3V3 S2 TRACKPAD VR (NEEDS REVIEW)

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```
84 PP3V3_S2_TPAD ═══ PP3V3_S2_TPAD
                     MAKE_BASE=TRUE
                     MIN_NECK_WIDTH=0.1000
                     MIN_LINE_WIDTH=0.2000
                     VOLTAGE=3.3
                     ═══ PP3V3_S2_TPAD   47
```

1V8 S2 SWITCH

```
39 PP1V8_S2SW_VDD1 ═══ PP1V8_S2SW_VDD1
                       MAKE_BASE=TRUE
                       MIN_NECK_WIDTH=0.1000
                       MIN_LINE_WIDTH=0.2000
                       VOLTAGE=1.8
                       ═══ PP1V8_S2SW_VDD1   10
                       ═══ PP1V8_S2SW_VDD1   97
                       ═══ PP1V8_S2SW_VDD1   93
```

1V8 AON LDO

```
35 PP1V8_AON ═══ PP1V8_AON   84 89
                 MAKE_BASE=TRUE
                 MIN_NECK_WIDTH=0.1000
                 MIN_LINE_WIDTH=0.2000
                 VOLTAGE=1.8V
                 ═══ PP1V8_AON   73 89
                 ═══ PP1V8_AON   92
                 ═══ PP1V8_AON   80
                 ═══ PP1V8_AON   23
                 ═══ PP1V8_AON   90
                 ═══ PP1V8_AON   98
                 ═══ PP1V8_AON   34
```

3V3 PANEL SWITCH

```
70 PP3V3_SW_LCD ═══ PP3V3_SW_LCD   41 6 89
                    MAKE_BASE=TRUE
                    MIN_NECK_WIDTH=0.1000
                    MIN_LINE_WIDTH=0.2000
                    VOLTAGE=3.3V
```

5V PANEL SWITCH

```
70 PP5V_SW_LCD ═══ PP5V_SW_LCD   69 89
                   MAKE_BASE=TRUE
                   MIN_NECK_WIDTH=0.1000
                   MIN_LINE_WIDTH=0.2000
                   VOLTAGE=5V
```

SYNC_MASTER=KEI_T668_MLB SYNC_DATE=11/06/2019

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POWER ALIASES 4

3V8 AON SENSE RESISTOR

44 PPBUS_VMAIN_VIN_ISNS

PPBUS_VMAIN_VIN_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.8

PPBUS_VMAIN_VIN_ISNS 24 25
PPBUS_VMAIN_VIN_ISNS 98

3V3 S2 VR HIGH SIDE SENSE RESISTOR

44 PPBUS_AON_3V3S2_VIN_ISNS

PPBUS_AON_3V3S2_VIN_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=13.1

PPBUS_AON_3V3S2_VIN_ISNS 38

5V S2 VR HIGH SIDE SENSE RESISTOR

44 PPBUS_AON_5VS2_VIN_ISNS

PPBUS_AON_5VS2_VIN_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=13.1

PPBUS_AON_5VS2_VIN_ISNS 36
PPBUS_AON_5VS2_VIN_ISNS 98

MASTER PMU HIGH SIDE SENSE RESISTOR

45 PP3V8_AON_MPMU_ISNS_VIN

PP3V8_AON_MPMU_ISNS_VIN
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.8

PP3V8_AON_MPMU_ISNS_VIN 31 33 34
PP3V8_AON_MPMU_ISNS_VIN 31
PP3V8_AON_MPMU_ISNS_VIN 99

SLAVE PMU HIGH SIDE SENSE RESISTOR

45 PP3V8_AON_SPMU_ISNS_VIN

PP3V8_AON_SPMU_ISNS_VIN
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.8

PP3V8_AON_SPMU_ISNS_VIN 27 28

ATC 3V3 LDO HIGH SIDE SENSE RESISTOR

45 PP3V8_AON_ATC_ISNS

PP3V8_AON_ATC_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.8

PP3V8_AON_ATC_ISNS 53
PP3V8_AON_ATC_ISNS 54

MESA HIGH SIDE SENSE RESISTOR

45 PP3V8_MESA_ISNS

PP3V8_MESA_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.8

PP3V8_MESA_ISNS 86

DFR 1.8/3.3V HIGH SIDE CURRENT SENSE (Ixxx)

45 PP3V8_AON_DFR_ISNS

PP3V8_AON_DFR_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.8

PP3V8_AON_DFR_ISNS 87
PP3V8_AON_DFR_ISNS 87

LEFT AMP SENSE RESISTOR

46 PPBUS_SPKRAMP_LEFT_ISNS

PPBUS_SPKRAMP_LEFT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=13.1

PPBUS_SPKRAMP_LEFT_ISNS 79
PPBUS_SPKRAMP_LEFT_ISNS 77
PPBUS_SPKRAMP_LEFT_ISNS 77

RIGHT AMP SENSE RESISTOR

46 PPBUS_SPKRAMP_RIGHT_ISNS

PPBUS_SPKRAMP_RIGHT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=13.1

PPBUS_SPKRAMP_RIGHT_ISNS 79
PPBUS_SPKRAMP_RIGHT_ISNS 78
PPBUS_SPKRAMP_RIGHT_ISNS 78

3V3 S2 WLANBT LOAD SIDE SENSE RESISTOR

46 PP3V3_S2_WLBT_ISNS

PP3V3_S2_WLBT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3

PP3V3_S2_WLBT_ISNS 62

USB2 LEVEL SHIFTER 3.3V (UF750) SENSE RESISTOR

46 PP3V3_S2SW_USBLS1_ISNS

PP3V3_S2SW_USBLS1_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3V

PP3V3_S2SW_USBLS1_ISNS 60

USB2 LEVEL SHIFTER 1.8V (UF750) SENSE RESISTOR

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46 PP1V8_S2_USBLS1_ISNS

PP1V8_S2_USBLS1_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.8

PP1V8_S2_USBLS1_ISNS 56 60

WLAN BT 1V8 S2 CURRENT SENSE (Ixxx)

46 PP1V8_S2_WLBT_ISNS

PP1V8_S2_WLBT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.8

PP1V8_S2_WLBT_ISNS 62

KEYBOARD 1.85V SENSE RESISTOR

6 PP1V85_S2_KBD_ISNS

PP1V85_S2_KBD_ISNS 89
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.85

PP1V85_S2_KBD_ISNS 82 83
PP1V85_S2_KBD_ISNS 82

KEYBOARD LED 5V SENSE RESISTOR

46 PP5V_S2_KBDLED_ISNS

PP5V_S2_KBDLED_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=5

PP5V_S2_KBDLED_ISNS 72

ALSCAM 5V SENSE RESISTOR

47 PP5V_S2_ALSCAM_ISNS

PP5V_S2_ALSCAM_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=5

PP5V_S2_ALSCAM_ISNS 6

TPAD 5V SENSE RESISTOR

47 PP5V_S2_TPAD_ISNS

PP5V_S2_TPAD_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=5

PP5V_S2_TPAD_ISNS 85

TPAD 3.3V RESISTOR

PP3V3_S2_TPAD_ISNS

PP3V3_S_TPAD_ISNS 89
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=5

PP3V3_S2_TPAD_ISNS 85

TPAD 1.85V SENSE RESISTOR

7 PP1V85_S2_TPAD_ISNS

PP1V85_S2_TPAD_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=5

PP1V85_S2_TPAD_ISNS 85

SYNC_MASTER=KEI_T668_MLB SYNC_DATE=09/12/2010

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TGA PCIE GP1 NC

8	NC PCIE USBHC D2R POS	NC PCIE USBHC D2R POS	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE USBHC D2R NEG	NC PCIE USBHC D2R NEG	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE USBHC R2D C POS	NC PCIE USBHC R2D C POS	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE USBHC R2D C NEG	NC PCIE USBHC R2D C NEG	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE CLK100M USBHC POS	NC PCIE CLK100M USBHC POS	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE CLK100M USBHC NEG	NC PCIE CLK100M USBHC NEG	MAKE_BASE=TRUE NO_TEST=1
8	NC USBHC RESET L	NC USBHC RESET L	MAKE_BASE=TRUE NO_TEST=1

TGA PCIE GP2 NC

8	NC PCIE ENET D2R POS	NC PCIE ENET D2R POS	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE ENET D2R NEG	NC PCIE ENET D2R NEG	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE ENET R2D C POS	NC PCIE ENET R2D C POS	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE ENET R2D C NEG	NC PCIE ENET R2D C NEG	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE CLK100M ENET POS	NC PCIE CLK100M ENET POS	MAKE_BASE=TRUE NO_TEST=1
8	NC PCIE CLK100M ENET NEG	NC PCIE CLK100M ENET NEG	MAKE_BASE=TRUE NO_TEST=1
8	NC ENET CLKREQ L	NC ENET CLKREQ L	MAKE_BASE=TRUE NO_TEST=1
8	NC ENET RESET L	NC ENET RESET L	MAKE_BASE=TRUE NO_TEST=1

TGA BOARD ID RESOLVE

	SPI DFR CS L	SPI DFR CS L	MAKE_BASE=TRUE 6 88

TGA SSPIO

6	NC SSPI0 MOSI	NC SSPI0 MOSI	MAKE_BASE=TRUE NO_TEST=1

TGA SOC I2S NC

6	NC SOC I2S1 MCK	NC SOC I2S1 MCK	MAKE_BASE=TRUE NO_TEST=1
6	NC SOC I2S0 MCK	NC SOC I2S0 MCK	MAKE_BASE=TRUE NO_TEST=1

TGA I2S3 NC

6	NC I2S3 BCLK	NC I2S3 BCLK	MAKE_BASE=TRUE NO_TEST=1
6	NC I2S3 D2R	NC I2S3 D2R	MAKE_BASE=TRUE NO_TEST=1
6	NC I2S3 R2D	NC I2S3 R2D	MAKE_BASE=TRUE NO_TEST=1
6	NC I2S3 LRCLK	NC I2S3 LRCLK	MAKE_BASE=TRUE NO_TEST=1
6	NC I2S3 MCLK	NC I2S3 MCLK	MAKE_BASE=TRUE NO_TEST=1

TGA ISP GPIOS NC

7	NC ISP GPIO1	NC ISP GPIO1	MAKE_BASE=TRUE NO_TEST=1
7	NC FTCAM RESET L	NC FTCAM RESET L	MAKE_BASE=TRUE NO_TEST=1

TGA SMC I2C RESOLVE

9	I2C SMC PWR SCL	I2C SMC PWR SCL	MAKE_BASE=TRUE 43 91
9	I2C SMC PWR SDA	I2C SMC PWR SDA	MAKE_BASE=TRUE 43 91
9	I2C SMC IPD SCL	I2C SMC IPD SCL	MAKE_BASE=TRUE 43
9	I2C SMC IPD SDA	I2C SMC IPD SDA	MAKE_BASE=TRUE 43

TGA DISPLAY NC & RESOLVE

7	NC SPI DISP BKLT MISO	NC SPI DISP BKLT MISO	MAKE_BASE=TRUE NO_TEST=1
7	NC SPI DISP BKLT MOSI R	NC SPI DISP BKLT MOSI R	MAKE_BASE=TRUE NO_TEST=1
7	NC DISP BKLT LSYNC	NC DISP BKLT LSYNC	MAKE_BASE=TRUE NO_TEST=1
7	NC BKLT FAULT INT L	NC BKLT FAULT INT L	MAKE_BASE=TRUE NO_TEST=1
41 7	I2C DISP BKLT SCL	I2C DISP BKLT SCL	MAKE_BASE=TRUE
41 7	I2C DISP BKLT SDA	I2C DISP BKLT SDA	MAKE_BASE=TRUE
7	NC DISPLAY POL	NC DISPLAY POL	MAKE_BASE=TRUE NO_TEST=1
7	NC DISP FSYNC	NC DISP SYNC	MAKE_BASE=TRUE NO_TEST=1
7	NC DISP TOUCH EB	NC DISP TOUCH EB	MAKE_BASE=TRUE NO_TEST=1
7	NC DISP TOUCH BSYNC0	NC DISP TOUCH BSYNC0	MAKE_BASE=TRUE NO_TEST=1
7	NC DISP TOUCH BSYNC1	NC DISP TOUCH BSYNC1	MAKE_BASE=TRUE NO_TEST=1
7	NC DISP SPMI CLK	NC DISP SPMI CLK	MAKE_BASE=TRUE NO_TEST=1
7	NC DISP SPMI DATA	NC DISP SPMI DATA	MAKE_BASE=TRUE NO_TEST=1

TGA AP GPIO NC & TP

6	NC SOC GPIO08	NC SOC GPIO08	MAKE_BASE=TRUE NO_TEST=1
6	TP SWD UPC SWDIO1	TP SWD UPC SWDIO1	MAKE_BASE=TRUE

TGA AOP GPIO NC & RESOLVE

9	NC R1 DUMP TRIG	NC R1 DUMP TRIG	MAKE_BASE=TRUE NO_TEST=1
9	NC AOP FUNC1	NC AOP FUNC1	MAKE_BASE=TRUE NO_TEST=1
9	NC R1 RTC SYNC	NC R1 RTC SYNC	MAKE_BASE=TRUE NO_TEST=1
9	NC R1 INT	NC R1 INT	MAKE_BASE=TRUE NO_TEST=1
9	NC SPI R1 CS L	NC SPI R1 CS L	MAKE_BASE=TRUE NO_TEST=1
9	NC AOP FUNC5	NC AOP FUNC5	MAKE_BASE=TRUE NO_TEST=1
	SPI GYRO CS L	SPI GYRO CS L	MAKE_BASE=TRUE 9 51
	GYRO INT	GYRO INT	MAKE_BASE=TRUE 9 51
	GYRO MOTION INT	GYRO MOTION INT	MAKE_BASE=TRUE 9 51
9	NC AOP FUNC10	NC AOP FUNC10	MAKE_BASE=TRUE NO_TEST=1
9	NC ALS INT L	NC ALS INT L	MAKE_BASE=TRUE NO_TEST=1
9	NC AOP FUNC14	NC AOP FUNC14	MAKE_BASE=TRUE NO_TEST=1

TGA AOP PDM NC

9	NC PDM CLK1	NC PDM CLK1	MAKE_BASE=TRUE NO_TEST=1
9	NC PDM DATA1	NC PDM DATA1	MAKE_BASE=TRUE NO_TEST=1
106 9	NC PDM CLK2	NC PDM CLK2	MAKE_BASE=TRUE NO_TEST=1 10
106 9	NC PDM CLK5	NC PDM CLK5	MAKE_BASE=TRUE NO_TEST=1 106
106 9	NC PDM CLK6	NC PDM CLK6	MAKE_BASE=TRUE NO_TEST=1 106
106 9	NC PDM DATA2	NC PDM DATA2	MAKE_BASE=TRUE NO_TEST=1 106

TGA AOP I2C

9	I2C AOP ALS SCL	I2C AOP ALS SCL	MAKE_BASE=TRUE 42
9	I2C AOP ALS SDA	I2C AOP ALS SDA	MAKE_BASE=TRUE 42

TGA AOP SPMI NC

9	NC AOP SPMI0 SCLK	NC AOP SPMI0 SCLK	MAKE_BASE=TRUE NO_TEST=1
9	NC AOP SPMI0 SDATA	NC AOP SPMI0 SDATA	MAKE_BASE=TRUE NO_TEST=1

TGA NUB & NUB GPIO & NUB SWD

	TP SOC DOCK ATTENTION	TP SOC DOCK ATTENTION	MAKE_BASE=TRUE 9 18
9	NC BKLT PWR ON SMC LED SEL	NC BKLT PWR ON SMC LED SEL	MAKE_BASE=TRUE NO_TEST=1
9	IPD SPI INT L	IPD SPI INT L	MAKE_BASE=TRUE 84
9	CHGR INT L	CHGR INT L	MAKE_BASE=TRUE 23
9	NC ENET I2C LOM INT L	NC ENET I2C LOM INT L	MAKE_BASE=TRUE NO_TEST=1
9	NC ACDC ID	NC ACDC ID	MAKE_BASE=TRUE NO_TEST=1
9	NC ACDC BURST EN L	NC ACDC BURST EN L	MAKE_BASE=TRUE NO_TEST=1
9	NC SPI DP2HDMI HOLD L	NC SPI DP2HDMI HOLD L	MAKE_BASE=TRUE NO_TEST=1
9	NC HDMI CEC AOP TX	NC HDMI CEC AOP TX	MAKE_BASE=TRUE NO_TEST=1
9	NC HDMI CEC AOP RX	NC HDMI CEC AOP RX	MAKE_BASE=TRUE NO_TEST=1
9	NC HDMI HPD AOP	NC HDMI HPD AOP	MAKE_BASE=TRUE NO_TEST=1
9	NC SWD NUB R1 SWDIO	NC SWD NUB R1 SWDIO	MAKE_BASE=TRUE NO_TEST=1

TGA MISC

5	NC SWD TMS3	NC SWD TMS3	MAKE_BASE=TRUE NO_TEST=1
8	NC NAND0 PCIE RESET1 L	NC NAND0 PCIE RESET1 L	MAKE_BASE=TRUE NO_TEST=1
6	PMU VDDHI UVWARN L	PMU VDDHI UVWARN L	MAKE_BASE=TRUE 33 34

TGA SPI

6	NC SOC SPI2 SSIN	NC SOC SPI2 SSIN	MAKE_BASE=TRUE NO_TEST=1

TGA GPIO NC

6	NC SOC GPIO01	NC SOC GPIO01	MAKE_BASE=TRUE NO_TEST=1
6	NC SOC GPIO15	NC SOC GPIO15	MAKE_BASE=TRUE NO_TEST=1
6	NC SOC GPIO16	NC SOC GPIO16	MAKE_BASE=TRUE NO_TEST=1
6	NC ENET SYNC 1588	NC ENET SYNC 1588	MAKE_BASE=TRUE NO_TEST=1

TGA SOC

18 5	TP SOC AMUX OUT	TP SOC AMUX OUT	MAKE_BASE=TRUE 89

TGA UART NC

6	NC UART3 D2R CTS L	NC UART3 D2R CTS L	MAKE_BASE=TRUE NO_TEST=1
6	NC UART3 R2D RTS L	NC UART3 R2D RTS L	MAKE_BASE=TRUE NO_TEST=1
6	NC UART3 D2R	NC UART3 D2R	MAKE_BASE=TRUE NO_TEST=1
6	NC UART3 R2D	NC UART3 R2D	MAKE_BASE=TRUE NO_TEST=1
6	NC UART4 D2R CTS L	NC UART4 D2R CTS L	MAKE_BASE=TRUE NO_TEST=1
6	NC UART4 R2D RTS L	NC UART4 R2D RTS L	MAKE_BASE=TRUE NO_TEST=1
6	NC UART4 D2R	NC UART4 D2R	MAKE_BASE=TRUE NO_TEST=1
6	NC UART4 R2D	NC UART4 R2D	MAKE_BASE=TRUE NO_TEST=1
6	NC UART7 RXD	NC UART7 RXD	MAKE_BASE=TRUE NO_TEST=1
6	NC UART7 TXD	NC UART7 TXD	MAKE_BASE=TRUE NO_TEST=1

TGA MIPI NC

7	NC MIPI0C CLK POS	NC MIPI0C CLK POS	MAKE_BASE=TRUE NO_TEST=1
7	NC MIPI0C CLK NEG	NC MIPI0C CLK NEG	MAKE_BASE=TRUE NO_TEST=1
7	NC MIPI0C DATA 0 POS	NC MIPI0C DATA 0 POS	MAKE_BASE=TRUE NO_TEST=1
7	NC MIPI0C DATA 0 NEG	NC MIPI0C DATA 0 NEG	MAKE_BASE=TRUE NO_TEST=1
7	NC MIPI0C DATA 1 POS	NC MIPI0C DATA 1 POS	MAKE_BASE=TRUE NO_TEST=1
7	NC MIPI0C DATA 1 NEG	NC MIPI0C DATA 1 NEG	MAKE_BASE=TRUE NO_TEST=1
7	NC MIPI FTCAM DATA POS1	NC MIPI FTCAM DATA POS1	MAKE_BASE=TRUE NO_TEST=1
	NC MIPI FTCAM DATA NEG1	NC MIPI FTCAM DATA NEG1	MAKE_BASE=TRUE NO_TEST=1

TGA LPDP AUX, TX NC

7	NC LPDPRX AUX0	NC LPDPRX AUX0	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDPRX AUX1	NC LPDPRX AUX1	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDPRX AUX2	NC LPDPRX AUX2	MAKE_BASE=TRUE NO_TEST=1
	NC LPDPRX AUX3	NC LPDPRX AUX3	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDPRX AUX4	NC LPDPRX AUX4	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDPRX AUX5	NC LPDPRX AUX5	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDPRX AUX6	NC LPDPRX AUX6	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDPRX AUX7	NC LPDPRX AUX7	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDPRX AUX8	NC LPDPRX AUX8	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDPRX AUX9	NC LPDPRX AUX9	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDPRX AUX10	NC LPDPRX AUX10	MAKE_BASE=TRUE NO_TEST=1
	NC LPDPRX AUX11	NC LPDPRX AUX11	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDP TX4POS	NC LPDP TX4POS	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDP TX4NEG	NC LPDP TX4NEG	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDP TX5POS	NC LPDP TX5POS	MAKE_BASE=TRUE NO_TEST=1
7	NC LPDP TX5NEG	NC LPDP TX5NEG	MAKE_BASE=TRUE NO_TEST=1

TGA ISP SPMI NC

7	NC ISP SPMI0 CLK	NC ISP SPMI0 CLK	MAKE_BASE=TRUE NO_TEST=1
7	NC ISP SPMI0 DATA	NC ISP SPMI0 DATA	MAKE_BASE=TRUE NO_TEST=1
	NC ISP SPMI1 CLK	NC ISP SPMI1 CLK	MAKE_BASE=TRUE NO_TEST=1
7	NC ISP SPMI1 DATA	NC ISP SPMI1 DATA	MAKE_BASE=TRUE NO_TEST=1
7	NC SENSOR1 CLK	NC SENSOR1 CLK	MAKE_BASE=TRUE NO_TEST=1
7	NC SENSOR2 CLK	NC SENSOR2 CLK	MAKE_BASE=TRUE NO_TEST=1
7	NC SENSOR3 CLK	NC SENSOR3 CLK	MAKE_BASE=TRUE NO_TEST=1
6	NC SPMI2 CLK	NC SPMI2 CLK	MAKE_BASE=TRUE NO_TEST=1

TGA MTR

8	NC MTR VREF NEG	NC MTR VREF NEG	MAKE_BASE=TRUE NO_TEST=1
8	NC MTR VREF POS	NC MTR VREF POS	MAKE_BASE=TRUE NO_TEST=1
8	NC MTR VREF ANAP	NC MTR VREF ANAP	MAKE_BASE=TRUE NO_TEST=1
8	NC MTR VREF ANAN	NC MTR VREF ANAN	MAKE_BASE=TRUE NO_TEST=1

TGA AOP I2CM1 NC

9	NC I2C AOP ENET SCL	NC I2C AOP ENET SCL	MAKE_BASE=TRUE NO_TEST=1
9	NC I2C AOP ENET SDA	NC I2C AOP ENET SDA	MAKE_BASE=TRUE NO_TEST=1

TGA PDM NC

106 9	NC PDM CLK2	NC PDM CLK2	MAKE_BASE=TRUE NO_TEST=1 106
106 9	NC PDM CLK5	NC PDM CLK5	MAKE_BASE=TRUE NO_TEST=1 106
106 9	NC PDM CLK6	NC PDM CLK6	MAKE_BASE=TRUE NO_TEST=1 106
106 9	NC PDM DATA2	NC PDM DATA2	MAKE_BASE=TRUE NO_TEST=1 106

TGA SMC GPIO NC & RESOLVE

9	NC SMC GPIO1	NC SMC GPIO1	MAKE_BASE=TRUE NO_TEST=1
52 9	SMC FAN PWM	SMC FAN PWM	MAKE_BASE=TRUE

TGA AOP UART2 NC

9	NC AOP UART2 D2R	NC AOP UART2 D2R	MAKE_BASE=TRUE NO_TEST=1
9	NC AOP UART2 R2D	NC AOP UART2 R2D	MAKE_BASE=TRUE NO_TEST=1

TGA ISP I2C0/1/3 NC

7	NC ISP I2C0 SCL	NC ISP I2C0 SCL	MAKE_BASE=TRUE NO_TEST=1
7	NC ISP I2C0 SDA	NC ISP I2C0 SDA	MAKE_BASE=TRUE NO_TEST=1
7	NC ISP I2C1 SCL	NC ISP I2C1 SCL	MAKE_BASE=TRUE NO_TEST=1
7	NC ISP I2C1 SDA	NC ISP I2C1 SDA	MAKE_BASE=TRUE NO_TEST=1
7	NC ISP I2C3 SCL	NC ISP I2C3 SCL	MAKE_BASE=TRUE NO_TEST=1
7	NC ISP I2C3 SDA	NC ISP I2C3 SDA	MAKE_BASE=TRUE NO_TEST=1

SYNC_MASTER=AITKEN_T668_MLB SYNC_DATE=09/18/2019

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LATTICE SECDIS FPGA

74	NC_SEP_IRCAM_DISABLE_IC_L	MAKE_BASE=TRUE	NC_SEP_IRCAM_DISABLE_IC_L NO_TEST=1
74	NC_IRCAM_ENABLE_IN_IC	MAKE_BASE=TRUE	NC_IRCAM_ENABLE_IN_IC NO_TEST=1
74	NC_IRCAM_ENABLE_SEC_1V8_OUT	MAKE_BASE=TRUE	NC_IRCAM_ENABLE_SEC_1V8_OUT NO_TEST=1
74	NC_DMIC_CLK2_IN_IC	MAKE_BASE=TRUE	NC_DMIC_CLK2_IN_IC NO_TEST=1
74	NC_DMIC_DATA2_1V8_IN	MAKE_BASE=TRUE	NC_DMIC_DATA2_1V8_IN NO_TEST=1
74	NC_DMIC_DATA2_SEC_OUT_IC	MAKE_BASE=TRUE	NC_DMIC_DATA2_SEC_OUT_IC NO_TEST=1
74	NC_FTCAM_ENABLE_IN	MAKE_BASE=TRUE	NC_FTCAM_ENABLE_IN NO_TEST=1
74	NC_FTCAM_ENABLE_SEC_1V8_OUT	MAKE_BASE=TRUE	NC_FTCAM_ENABLE_SEC_1V8_OUT NO_TEST=1
74	NC_DMIC_CLK2_1V8_OUT_R_IC	MAKE_BASE=TRUE	NC_DMIC_CLK2_1V8_OUT_R_IC

ACE2 GPIOS

57 55	UPC_SMC_I2C_INT_L	MAKE_BASE=TRUE	UPC_SMC_I2C_INT_L
58	UPC_SMC_I2C_INT_L		
57 55	UPC_I2C_INT_L	MAKE_BASE=TRUE	UPC_I2C_INT_L 6
58	UPC_I2C_INT_L		
56	UPC0_GPIO7	MAKE_BASE=TRUE	UPC0_GPIO7 56 57 96

TGA LPDP RX NC

7	NC_LPDPRX_RX_P_0	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_0 NO_TEST=1
7	NC_LPDPRX_RX_N_0	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_0 NO_TEST=1
7	NC_LPDPRX_RX_P_1	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_1 NO_TEST=1
7	NC_LPDPRX_RX_N_1	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_1 NO_TEST=1
7	NC_LPDPRX_RX_P_2	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_2 NO_TEST=1
7	NC_LPDPRX_RX_N_2	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_2 NO_TEST=1
7	NC_LPDPRX_RX_P_3	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_3 NO_TEST=1
7	NC_LPDPRX_RX_N_3	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_3 NO_TEST=1
7	NC_LPDPRX_RX_P_4	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_4 NO_TEST=1
7	NC_LPDPRX_RX_N_4	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_4 NO_TEST=1
7	NC_LPDPRX_RX_P_5	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_5 NO_TEST=1
7	NC_LPDPRX_RX_N_5	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_5 NO_TEST=1
7	NC_LPDPRX_RX_P_6	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_6 NO_TEST=1
7	NC_LPDPRX_RX_N_6	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_6 NO_TEST=1
7	NC_LPDPRX_RX_P_7	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_7 NO_TEST=1
7	NC_LPDPRX_RX_N_7	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_7 NO_TEST=1
7	NC_LPDPRX_RX_P_8	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_8 NO_TEST=1
7	NC_LPDPRX_RX_N_8	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_8 NO_TEST=1
7	NC_LPDPRX_RX_P_9	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_9 NO_TEST=1
7	NC_LPDPRX_RX_N_9	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_9 NO_TEST=1
7	NC_LPDPRX_RX_P_10	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_10 NO_TEST=1
7	NC_LPDPRX_RX_N_10	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_10 NO_TEST=1
7	NC_LPDPRX_RX_P_11	MAKE_BASE=TRUE	NC_LPDPRX_RX_P_11 NO_TEST=1
7	NC_LPDPRX_RX_N_11	MAKE_BASE=TRUE	NC_LPDPRX_RX_N_11 NO_TEST=1

USB LEVEL SHIFTER

60	TP_EUSB_LS1NEG	MAKE_BASE=TRUE	TP_EUSB_LS1NEG
60	TP_EUSB_LS1POS	MAKE_BASE=TRUE	TP_EUSB_LS1POS
60	NC_USB_LS1NEG	MAKE_BASE=TRUE	NC_USB_LS1NEG 107
60	NC_USB_LS1POS	MAKE_BASE=TRUE	NC_USB_LS1POS 107
96 60	USB2_ATC0_LS_MUX_P	MAKE_BASE=TRUE	USB2_ATC0_LS_MUX_P
96 60	USB2_ATC0_LS_MUX_N	MAKE_BASE=TRUE	USB2_ATC0_LS_MUX_N
96 60	USB_DBG_LS_MUX_P	MAKE_BASE=TRUE	USB_DBG_LS_MUX_P
96 60	USB_DBG_LS_MUX_N	MAKE_BASE=TRUE	USB_DBG_LS_MUX_N
60	USB2_ATC1_LS_P	MAKE_BASE=TRUE	USB2_ATC1_LS_P 61
60	USB2_ATC1_LS_N	MAKE_BASE=TRUE	USB2_ATC1_LS_N 61
107	NC_USB_LS1POS	MAKE_BASE=TRUE	NC_USB_LS1POS
107	NC_USB_LS1NEG	MAKE_BASE=TRUE	NC_USB_LS1NEG

AUDIO AMPLIFIER TDM

75	TDM_1V8_SPKRAMP_L_BCLK	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_BCLK 77 80
			TDM_1V8_SPKRAMP_L_BCLK 77
75	TDM_1V8_SPKRAMP_L_FSYNC	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_FSYNC 77 80
			TDM_1V8_SPKRAMP_L_FSYNC 77
75	TDM_1V8_SPKRAMP_L_R2D	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_R2D 77 80
			TDM_1V8_SPKRAMP_L_R2D 77
75	TDM_1V8_SPKRAMP_L_D2R	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_D2R 77 80
			TDM_1V8_SPKRAMP_L_D2R 77
75	TDM_1V8_SPKRAMP_R_BCLK	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_BCLK 78 8
			TDM_1V8_SPKRAMP_R_BCLK 78
75	TDM_1V8_SPKRAMP_R_FSYNC	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_FSYNC 78 80
			TDM_1V8_SPKRAMP_R_FSYNC 78
75	TDM_1V8_SPKRAMP_R_R2D	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_R2D 78 80
			TDM_1V8_SPKRAMP_R_R2D 78
75	TDM_1V8_SPKRAMP_R_D2R	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_D2R 78 80
			TDM_1V8_SPKRAMP_R_D2R 78

SPEAKERAMP RESET

75	SPKRAMP_RESET_L	MAKE_BASE=TRUE	SPKRAMP_RESET_L 6

USBC LDO ENABLES

53	USBC0_3V3LDO_EN_MUX	MAKE_BASE=TRUE	USBC0_3V3LDO_EN_MUX
96	USBC0_3V3LDO_EN_MUX		
54	USBC1_3V3LDO_EN	MAKE_BASE=TRUE	USBC1_3V3LDO_EN 58

USBC LDO HPD

5	NC_ATC1_HPD	MAKE_BASE=TRUE	NC_ATC1_HPD NO_TEST=1
5	NC_ATC0_HPD	MAKE_BASE=TRUE	NC_ATC0_HPD NO_TEST=1

CHARGER

22	NC_CHGR_EN_VR1	MAKE_BASE=TRUE	NC_CHGR_EN_VR1 NO_TEST=1

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NAND REFERENCE

64	SWD_NAND0_SWCLK	MAKE_BASE=TRUE	SWD_NAND0_SWCLK 5 67 107
64	SWD_NAND0_SWDIO	MAKE_BASE=TRUE	SWD_NAND0_SWDIO 5 67 107
65	SWD_NAND0_SWCLK	MAKE_BASE=TRUE	SWD_NAND0_SWCLK 5 67 107
65	SWD_NAND0_SWDIO	MAKE_BASE=TRUE	SWD_NAND0_SWDIO 5 67 107
64	PP0V9_S5E0_VDD_PLL	MAKE_BASE=TRUE	PP0V9_S5E0_VDD_PLL 67
65	PP0V9_S5E1_VDD_PLL	MAKE_BASE=TRUE	PP0V9_S5E1_VDD_PLL 67

SE

20	NC_I2C_SE_SCL	MAKE_BASE=TRUE	NC_I2C_SE_SCL NO_TEST=1
20	NC_I2C_SE_SDA	MAKE_BASE=TRUE	NC_I2C_SE_SDA NO_TEST=1

DISPLAY POWER SEQUENCER

70	PMU_SYS_ALIVE	MAKE_BASE=TRUE	PMU_SYS_ALIVE 33 67 89 100

VITAMIN C

96	NC_DEBUG_JTAG_SOC_TDO	MAKE_BASE=TRUE	NC_DEBUG_JTAG_SOC_TDO NO_TEST=1
96	NC_DEBUG_JTAG_SOC_TDI	MAKE_BASE=TRUE	NC_DEBUG_JTAG_SOC_TDI NO_TEST=1
96	NC_DC_MUX_SEL	MAKE_BASE=TRUE	NC_DC_MUX_SEL NO_TEST=1
96 60	ATCRTMR0_RESET_MUX_1V8_L	MAKE_BASE=TRUE	ATCRTMR0_RESET_MUX_1V8_L

USBC CIO

53	USBC_ATC0_R2D_P<1>	MAKE_BASE=TRUE	USBC_ATC0_R2D_P<1> 53
53	USBC_ATC0_R2D_N<1>	MAKE_BASE=TRUE	USBC_ATC0_R2D_N<1> 53
53	USBC_ATC0_R2D_P<2>	MAKE_BASE=TRUE	USBC_ATC0_R2D_P<2> 53
53	USBC_ATC0_R2D_N<2>	MAKE_BASE=TRUE	USBC_ATC0_R2D_N<2> 53
53	USBC_ATC0_D2R_C_P<1>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_P<1> 53
53	USBC_ATC0_D2R_C_N<1>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_N<1> 53
53	USBC_ATC0_D2R_C_P<2>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_P<2> 53
53	USBC_ATC0_D2R_C_N<2>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_N<2> 53
54	USBC_ATC1_R2D_P<1>	MAKE_BASE=TRUE	USBC_ATC1_R2D_P<1> 54
54	USBC_ATC1_R2D_N<1>	MAKE_BASE=TRUE	USBC_ATC1_R2D_N<1> 54
54	USBC_ATC1_R2D_P<2>	MAKE_BASE=TRUE	USBC_ATC1_R2D_P<2> 54
54	USBC_ATC1_R2D_N<2>	MAKE_BASE=TRUE	USBC_ATC1_R2D_N<2> 54
54	USBC_ATC1_D2R_C_P<1>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_P<1> 54
54	USBC_ATC1_D2R_C_N<1>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_N<1> 54
54	USBC_ATC1_D2R_C_P<2>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_P<2> 54
54	USBC_ATC1_D2R_C_N<2>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_N<2> 54

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53	USBC0_D2R_P<1>	MAKE_BASE=TRUE	USBC0_D2R_P<1> 59
53	USBC0_D2R_N<1>	MAKE_BASE=TRUE	USBC0_D2R_N<1> 59
53	USBC0_D2R_P<2>	MAKE_BASE=TRUE	USBC0_D2R_P<2> 59
53	USBC0_D2R_N<2>	MAKE_BASE=TRUE	USBC0_D2R_N<2> 59
53	USBC0_R2D_CR_P<1>	MAKE_BASE=TRUE	USBC0_R2D_CR_P<1> 59
53	USBC0_R2D_CR_N<1>	MAKE_BASE=TRUE	USBC0_R2D_CR_N<1> 59
53	USBC0_R2D_CR_P<2>	MAKE_BASE=TRUE	USBC0_R2D_CR_P<2> 59
53	USBC0_R2D_CR_N<2>	MAKE_BASE=TRUE	USBC0_R2D_CR_N<2> 59
54	USBC1_D2R_P<1>	MAKE_BASE=TRUE	USBC1_D2R_P<1> 59
54	USBC1_D2R_N<1>	MAKE_BASE=TRUE	USBC1_D2R_N<1> 59
54	USBC1_D2R_P<2>	MAKE_BASE=TRUE	USBC1_D2R_P<2> 59
54	USBC1_D2R_N<2>	MAKE_BASE=TRUE	USBC1_D2R_N<2> 59
54	USBC1_R2D_CR_P<1>	MAKE_BASE=TRUE	USBC1_R2D_CR_P<1> 59
54	USBC1_R2D_CR_N<1>	MAKE_BASE=TRUE	USBC1_R2D_CR_N<1> 59
54	USBC1_R2D_CR_P<2>	MAKE_BASE=TRUE	USBC1_R2D_CR_P<2> 59
54	USBC1_R2D_CR_N<2>	MAKE_BASE=TRUE	USBC1_R2D_CR_N<2> 59

USBC0 LANE SWAP

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SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from stackup. Shortest distance is used unless '_' is defined	EXAMPLE 1,2,3,4,5,6,10, 2-10
A_DIELECTRIC_(N)XD XV,XVL,X Calculates dielectric distance from shortest table and stackup. Shortest distance is used unless '_' defined	EXAMPLE 2,10,20,30,40,50,100, PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from stackup. Shortest distance is used unless '_' is defined	EXAMPLE 2,4,6,8, 2-10

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17.2 RULES

PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR DOMINEERING
CLASS NAME	PRIM CLASS	CONSTRAINT SET	DP NAMES EX: DP:DP AA*,DP BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	P	A_45_OHM_SE	*SMB*SCL*,*SMB*SDA*,*I2C*SCL*,*I2C*SDA*,*I2C*INT*	Y
SPI	P	A_45_OHM_SE	*SPI*MISO*,*SPI*MOSI*,*SPI*CLK*,*SPI*CS*	Y
SPMI	P	A_45_OHM_SE	*SPMI*	Y
SWD	P	A_45_OHM_SE	SWD_NAND*,SWD_NUB*	Y
JTAG	P	A_45_OHM_SE	*JTAG*SEL,*JTAG*TCK,*JTAG*TDI,*JTAG*TDO,*JTAG*TMS	Y
CLOCK_24M	P	A_45_OHM_SE	SOC_24M_O_R,NAND0_CLK24M*	Y
SOC_XTAL_24M_IN	P	A_45_OHM_SE	SOC_XTAL24M_IN	Y
SOC_XTAL_24M_OUT	P	A_45_OHM_SE	SOC_XTAL24M_OUT	Y
CLOCK_32K	P	A_45_OHM_SE	PMU_CLK32K*	Y
TDM_LEFT	P	A_45_OHM_SE	TDM_SPKRAMP_L*.TDM_SPKRAMP_A*,TDM_SPKRAMP_B*	Y
TDM_RIGHT	P	A_45_OHM_SE	TDM_SPKRAMP_R*,TDM_SPKRAMP_D*,TDM_SPKRAMP_E*	Y
TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
SPKR_ICC	P	A_45_OHM_SE	SPKRAMP_ICC,SPKRAMP_*_ICC_R	Y
UART	P	A_45_OHM_SE	UART_*	Y
RESETS	P	A_45_OHM_SE	*RST*,*RESET*,*PERST*,!PP3V3_UPC_PMU_RESET_R	Y
WDOG	P	A_45_OHM_SE	SOC_WDOG	Y
SOCHOT	P	A_45_OHM_SE	SOC_SOCHOT_L	Y
POWER_BUTTON	P	A_45_OHM_SE	*PMU_ONOFF*	Y
FAULT	P	A_45_OHM_SE	*FAULT*,!FAULT_LED_RST_L	Y
DMIC PDM	P	A 45 OHM SE	PDM_DMIC_DATA*,DMIC_DATA*,PDM_DMIC_CLK*,DMIC_CLK*	Y
FAN_CTRL	P	A_45_OHM_SE	SMC_FAN_*	Y
USBC_SOC_BSB0_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_D2R_C_1	Y
USBC_SOC_BSB0_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_D2R_C_2	Y
USBC_SOC_BSB0_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_R2D_1	Y
USBC SOC BSB0 R2D 2	P	A 85 OHM DIFF	DP:DP USBC ATC0 R2D 2	Y
USBC_SOC_BSB0_AUX	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_AUX	Y
USBC_SOC_BSB0_LSX	P	A_45_OHM_SE	CIO_ATC0_LS*	Y
USBC_BSB0_CONN_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC0_D2R_CR_1	Y
USBC_BSB0_CONN_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC0_D2R_CR_2	Y
USBC_BSB0_CONN_R2D_1	P	A 85 OHM DIFF	DP:DP USBC0 R2D C 1	Y
USBC_BSB0_CONN_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC0_R2D_C_2	Y
USBC_BSB0_CONN_AUXLSX	P	A_85_OHM_DIFF	DP:DP_USBC0_AUXLSX	Y
USBC_UPC0_CONN_TOP	P	A_85_OHM_DIFF	DP:DP_U BC0_USB_TOP	Y
USBC_UPC0_CONN_BOT	P	A_85_OHM_DIFF	DP:DP_USBC0_USB_BOT	Y
USBC_UPC0_CONN_CC	P	WIDTH_0P400	USBC0_CC*	Y
USBC_UPC0_CONN_SBU	P	A_45_OHM_SE	USBC0_SBU*	Y
USBC_SOC_RTMR0_USB2	P	A_85_OHM_DIFF_TIGHT	DP:DP_EUSB_ATC0	Y
USBC_RTMR0_MUX_USB2	P	A_85_OHM_DIFF_TIGHT	DP:DP_USB2_ATC0_LS_MUX	Y
USBC_MUX_UPC0_USB2	P	A_85_OHM_DIFF_TIGHT	DP:DP_USB2_ATC0_LS,DP_USB2_ATC0_LS_R	Y
USBC_MUX_VITC_USB2	P	A_85_OHM_DIFF_TIGHT	DP:DP_USB2_ATC0_LS_VITAMINC	Y
USBC_SOC_BSB1_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_D2R_C_1	Y
USBC_SOC_BSB1_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_D2R_C_2	Y
USBC_SOC_BSB1_R2D_1	P	A_85_OHM_DIFF	DP:DP_US C_ATC1_R2D_1	Y
USBC_SOC_BSB1_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_R2D_2	Y
USBC_SOC_BSB1_AUX	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_AUX	Y
USBC_SOC_BSB1_LSX	P	A_45_OHM_SE	CIO_ATC1_LS*	Y
USBC_BSB1_CONN_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC1_D2R_CR_1	Y
USBC_BSB1_CONN_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC1_D2R_CR_2	Y
USBC_BSB1_CONN_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC1_R2D_C_1	Y
USBC BSB1 CONN R2D 2	P	A_85_OHM_DIFF	DP:DP_USBC1_R2D_C_2	Y
USBC_BSB1_CONN_AUXLSX	P	A_85_OHM_DIFF	DP:DP_USBC1_AUXLSX	Y
USBC_UPC1_CONN_TOP	P	A_85_OHM_DIFF	DP:DP_USBC1_USB_TOP	Y
USBC_UPC1_CONN_BOT	P	A_85_OHM_DIFF	DP:DP_U BC1_USB_BOT	Y
USBC_UPC1_CONN_CC	P	WIDTH_0P400	USBC1_CC*	Y
USBC_UPC1_CONN_SBU	P	A_45_OHM_SE	USBC1 SBU*	Y
USBC_SOC_RTMR1_USB2	P	A_85_OHM_DIFF_TIGHT	DP:DP_EUSB_ATC1	Y
USBC_RTMR1 UPC1_USB2	P	A_85_OHM_DIFF_TIGHT	DP:DP_USB2_ATC1_LS	Y
USBC_SOC_RTMR_USB2_DBG	P	A_85_OHM_DIFF_TIGHT	DP:DP_EUSB_DBG	Y
USBC_RTMR_MUX_USB2_DBG	P	A_85_OHM_DIFF_TIGHT	DP:DP_USB_DBG_LS_MUX	Y
USBC_MUX_UPC_USB2_DBG	P	A 85 OHM DIFF TIGHT	DP:DP_USB_DBG_LS,DP_USB_DBG_LS_R	Y
USBC_MUX_VITC_USB2_DBG	P	A_85_OHM_DIFF_TIGHT	DP:DP_USB_DBG_LS_VITAMINC	Y
USBC_LSX	P	A_45_OHM_SE	*ATC*LS*X	Y
MIPI_FTCAM_CLK	P	A_85_OHM_DIFF_TIGHT	DP:DP_MIPI_FTCAM_CLK,DP_MIPI_CLOCK_CONN	Y
MIPI_FTCAM_DATA	P	A_85_OHM_DIFF_TIGHT	DP:DP_MIPI_FTCAM_DATA_0,DP_MIPI_DATA_CONN	Y
MIPI_DFR_CLK	P	A_85_OHM_DIFF_TIGHT	DP:DP_MIPI_DFR_CLK_CONN_FILT	Y
MIPI_DFR_DATA	P	A_85_OHM_DIFF_TIGHT	DP:DP_MIPI_DFR_DATA_CONN_FILT	Y
PCIE_WIFI_D2R	P	A_85_OHM_DIFF_TIGHT	DP:DP_PCIE_WLBT_D2R_C	Y
PCIE_WIFI_R2D	P	A_85_OHM_DIFF_TIGHT	DP:DP_PCIE_WLBT_R2D_C	Y
PCIE_WIFI_CLK	P	A_85_OHM_DIFF_TIGHT	DP:DP_PCIE_CLK100M_WLBT	Y
PCIE_NAND0_D2R	P	A 85 OHM DIFF TIGHT	DP:DP_PCIE_NAND0_D2R_C_0	Y
PCIE_NAND0_R2D	P	A_85_OHM_DIFF_TIGHT	DP:DP_PCIE_NAND0_R2D_C_0	Y
PCIE_NAND0_CLK	P	A_85_OHM_DIFF_TIGHT	DP:DP_PCIE_CLK100M_NAND0_0	Y
PCIE_NAND1_D2R	P	A_85_OHM_DIFF_TIGHT	DP:DP_PCIE_NAND0_D2R_C_1	Y
PCIE_NAND1_R2D	P	A_85_OHM_DIFF_TIGHT	DP:DP_PCIE_NAND0_R2D_C_1	Y
PCIE_NAND1_CLK	P	A 85 OHM DIFF TIGHT	DP:DP_PCIE_CLK100M_NAND0_1	Y
PCIE_CLKREQ	P	A_45_OHM_SE	*CLKREQ*	Y
PANEL_L DP_DATA	P	A_85_OHM_DIFF_TIGHT	DP:DP_DP0,DP_DP1,DP_DP2,DP_DP3	Y
PANEL_L DP_AUX	P	A_85_OHM_DIFF_TIGHT	DP:DP_AUX	Y
RCAL_PCIE	P	WIDTH_0P100	SOC_ST_PCIE_RCAL*,SOC_GP_PCIE_RCAL*	Y
RCAL_CIO	P	WIDTH 0P100	SOC_ATCPHY0_RCAL*,SOC_ATCPHY1_RCAL*	Y
RCAL_MIPI	P	WIDTH_0P100	*MIPI*REXT	Y
RCAL_EUSB	P	WIDTH_0P100	SOC_ATC*_USB_RESREF,SOC_USBDBG_RESREF	Y
BOARD_ID	P	A_45_OHM_SE	BO RD_ID*	Y
BOARD_REV	P	A_45_OHM_SE	BOARD_REV*	Y
WIRELESS_TIME_SYNC	P	A_45_OHM_SE	*TIME_SYNC*	Y
KBD_PWM	P	A_45_OHM_SE	*KBD_BKLT_PWM*,BKLT_PWM_KEYB_3V3	Y

PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR DOMINEERING
CLASS NAME	PRIM CLASS	CONSTRAINT SET	DP NAMES EX: DP:DP AA*,DP BB* (LINE STARTS WITH FLAG DP:)	Y/N
GROUND	P	DEFAULT	GND	Y
ANALOG_GROUND	P	DEFAULT	*AGND*,GND_*	Y
AUDIO_CONN_HEADPHONE_OUT	P	WIDTH_0P400	UDIO_JACK_LEFT_OUT,AUDIO_JACK_RIGHT_OUT	Y
AUDIO_CONN_HEADPHONE_OUT	P	WIDTH_0P400	AUD_CONN_LEFT_OUT,AUD_CONN_RIGHT_OUT	Y
AUDIO_CONN_RETURN	P	WIDTH_0P500	AUDIO_JACK_GB_GND,AUDIO_JACK_CH_GND	Y
AUDIO_CONN_RETURN	P	WIDTH_0P500	AUD_CONN_RING2,AUD_CONN_SLEEVE	Y
AUDIO_CONN_SENSE	P	WIDTH_0P100	AUDIO_JACK_LEFT_SNS,AUDIO_JACK_RIGHT_SNS	Y
AUDIO_CONN_SENSE	P	WIDTH_0P100	AUDIO_JACK_TIP_SNS,AUDIO_JACK_RING_SNS	Y
AUDIO_CONN_SENSE	P	WIDTH_0P100	AUD_CONN_LEFT_SNS,AUD_CONN_RIGHT_SNS	Y
AUDIO_CONN_SENSE	P	WIDTH_0P100	AUD_CONN_TIP_SENSE,AUD_CONN_RING_SENSE	Y
SPEAKERAMP_OUTPUT	P	SPKRAMP_OUT_DIFF	DP:DP_SPKRAMP_*_OUT	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_CHGR_CS*,DP_ISNS_*,DP_*VSNS_XW,DP_*_VSEN_XW	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_SPMU_TDEV,DP_SPKRAMP_*_VSENSE	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_P3V8AON_ISEN*,DP_THMSNS*,DP_ISNS_*LCD	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_SOC_*_RCAL,DP_P3V8IDIF2_FB	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_P3V8AON_VSNS,DP_ATCRTMR*_THERM_D	Y
RF_ANTENNA	P	WIDTH_0P100	RF_ANT_0,RF_ANT_1	Y
PMU_BUCK_FB	P	VR_FEEDBACK	BUCK*_FB*	Y
POWER	P	POWER	PP*	Y
CAPSLOCK_LED	P	WIDTH_0P150	KBD_CAP_CATHODE,KBD_LED1	Y
DBGLED_RETURN	P	WIDTH_0P200	DBGLED_RETURN	Y

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17.2 PHYSICAL CSETS

SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR PARENTS
CLASS NAME	TYPE	CONSTRAINT SET	DP NAMES EX: DP:DP AA*,DP BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	S	A_DIELECTRIC_3X	=	Y
SPI	S	A_DIELECTRIC_3X	=	Y
SPMI	S	A_DIELECTRIC_3X	=	Y
SWD	S	A_DIELECTRIC_3X		Y
JTAG	S	A DIELECTRIC 2X	=	Y
CLOCK_24M	S	A_DIELECTRIC_8X	=	Y
SOC_XTAL_24M_IN	S	A_DIELECTRIC_8X	=	Y
SOC_XTAL_24M_OUT	S	A_DIELECTRIC_8X	=	Y
CLOCK_32K	S	A_DIELECTRIC_8X	=	Y
TDM LEFT	S	A DIELECTRIC 3X	=	Y
TDM_RIGHT	S	A_DIELECTRIC_3X	=	Y
TDM_CODEC	S	A_DIELECTRIC_3X	=	Y
SPKR_ICC	S	A_DIELECTRIC_3X	=	Y
UART	S	A_DIELECTRIC_2X		Y
RESETS	S	A DIELECTRIC 3X	=	Y
WDOG	S	A_DIELECTRIC_3X	=	Y
SOCHOT	S	A_DIELECTRIC_3X	=	Y
POWER_BUTTON	S	A_DIELECTRIC_3X	=	Y
FAULT	S	A_DIELECTRIC_3X	=	Y
DMIC_PDM	S	A DIELECTRIC 3X	=	Y
FAN_CTRL	S	A_DIELECTRIC_2X	=	Y
USBC_SOC_BSB0_D2R_1	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_D2R_2	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_R2D_1	S	A_DIELECTRIC_9X		Y
USBC SOC BSB0 R2D 2	S	A DIELECTRIC 9X	=	Y
USBC_SOC_BSB0_AUX	S	A_DIELECTRIC_7X	=	Y
USBC_SOC_BSB0_LSX	S	A_DIELECTRIC_7X	=	Y
USBC_BSB0_CONN_D2R_1	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_D2R_2	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_R2D_1	S	A DIELECTRIC 9X	=	Y
USBC_BSB0_CONN_R2D_2	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_AUXLSX	S	A_DIELECTRIC_7X	=	Y
USBC_UPC0_CONN_TOP	S	A_DIELECTRIC_5X	=	Y
USBC_UPC0_CONN_BOT	S	A_DIELECTRIC_5X		Y
USBC_UPC0_CONN_CC	S	A_DIELECTRIC_2X	=	Y
USBC_UPC0_CONN_SBU	S	A_DIELECTRIC_2X	=	Y
USBC_SOC_RTMR0_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_RTMR0_MUX_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_UPC0_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_VITC_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_SOC_BSB1_D2R_1	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_D2R_2	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_R2D_1	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_R2D_2	S	A_DIELECTRIC_10X		Y
USBC_SOC_BSB1_AUX	S	A_DIELECTRIC_7X	=	Y
USBC_SOC_BSB1_LSX	S	A_DIELECTRIC_7X	=	Y
USBC_BSB1_CONN_D2R_1	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_D2R_2	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_R2D_1	S	A_DIELECTRIC_10X	=	Y
USBC BSB1 CONN R2D 2	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_AUXLSX	S	A_DIELECTRIC_7X	=	Y
USBC_UPC1_CONN_TOP	S	A_DIELECTRIC_5X	=	Y
USBC_UPC1_CONN_BOT	S	A_DIELECTRIC_5X	=	Y
USBC_UPC1_CONN_CC	S	A_DIELECTRIC_2X		Y
USBC UPC1 CONN SBU	S	A_DIELECTRIC_2X	=	Y
USBC_SOC_RTMR1_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_RTMR1_UPC1_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_SOC_RTMR_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_RTMR_MUX_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC MUX UPC USB2 DBG	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_VITC_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_LSX	S	A_DIELECTRIC_6X	=	Y
MIPI_FTCAM_CLK	S	A_DIELECTRIC_6X	=	Y
MIPI_FTCAM_DATA	S	A_DIELECTRIC_6X		Y
MIPI DFR CLK	S	A DIELECTRIC 6X	=	Y
MIPI_DFR_DATA	S	A_DIELECTRIC_6X	=	Y
PCIE_WIFI_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_WIFI_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_WIFI_CLK	S	A_DIELECTRIC_7X	=	Y
PCIE NAND0 D2R	S	A DIELECTRIC 7X	=	Y
PCIE_NAND0_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND0_CLK	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND1_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND1_R2D	S	A_DIELECTRIC_7X		Y
PCIE_NAND1_CLK	S	A DIELECTRIC 7X	=	Y
PCIE_CLKREQ	S	A_DIELECTRIC_2X	=	Y
PANEL_LPDP_DATA	S	A_DIELECTRIC_6X	=	Y
PANEL_LPDP_AUX	S	A_DIELECTRIC_6X	=	Y
RCAL_PCIE	S	A_DIELECTRIC_2X	=	Y
	S	A DIELECTRIC 2X	=	Y
RCAL_MIPI	S	A_DIELECTRIC_2X	=	Y
RCAL_EUSB	S	A_DIELECTRIC_2X	=	Y
BOARD_ID	S	A_DIELECTRIC_2X	=	Y
BOARD_REV	S	A_DIELECTRIC_2X		Y
WIRELESS TIME SYNC	S	A DIELECTRIC 2X	=	Y
KBD_PWM	S	A_DIELECTRIC_2X	=	Y
GROUND	S	DEFAULT	=	Y
ANALOG_GROUND	S	DEFAULT	=	Y

SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR PARENTS
CLASS NAME	TYPE	CONSTRAINT SET	DP NAMES EX: DP:DP AA*,DP BB* (LINE STARTS WITH FLAG DP:)	Y/N
AUDIO_CONN_HEADPHONE_OUT	S	A_DIELECTRIC_3X	=	Y
AUDIO_CONN_RETURN	S	A_DIELECTRIC_2X	=	Y
AUDIO_CONN_SENSE	S	A_DIELECTRIC_2X	=	Y
SPEAKERAMP_OUTPUT	S	A_DIELECTRIC_2X	=	Y
SENSE DIFF	S	A DIELECTRIC 2X	=	Y
RF_ANTENNA	S	RF_ANTENNA	=	Y
PMU_BUCK_FB	S	DEFAULT	=	Y
	S	DEFAULT	=	Y
CAPSLOCK_LED	S	DEFAULT	=	Y
DBGLED RETURN	S	DEFAULT	=	Y

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17.2 SPACING CSETS, ISO

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	GROUND	DEFAULT
SPI	GROUND	DEFAULT
SPMI	GROUND	DEFAULT
SWD	GROUND	DEFAULT
JTAG	GROUND	DEFAULT
CLOCK_24M	GROUND	DEFAULT
CLOCK_32K	GROUND	DEFAULT
TDM_LEFT	GROUND	DEFAULT
TDM_RIGHT	GROUND	DEFAULT
TDM_CODEC	GROUND	DEFAULT
SPKR_ICC	GROUND	DEFAULT
UART	GROUND	DEFAULT
RESETS	GROUND	DEFAULT
WDOG	GROUND	DEFAULT
SOCHOT	GROUND	DEFAULT
POWER_BUTTON	GROUND	DEFAULT
FAULT	GROUND	DEFAULT
DMIC_PDM	GROUND	DEFAULT
FAN_CTRL	GROUND	DEFAULT
USBC_SOC_BSB0_D2R_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_D2R_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_R2D_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_R2D_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_AUX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_LSX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_D2R_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_D2R_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_R2D_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_R2D_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_AUXLSX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_TOP	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_BOT	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_CC	GROUND	DEFAULT
USBC_UPC0_CONN_SBU	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR0_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR0_MUX_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_UPC0_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_VITC_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_D2R_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_D2R_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_R2D_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_R2D_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_AUX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_LSX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_D2R_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_D2R_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_R2D_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_R2D_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_AUXLSX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_TOP	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_BOT	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_CC	GROUND	DEFAULT
USBC_UPC1_CONN_SBU	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR1_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR1_UPC1_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR_USB2_DBG	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR_MUX_USB2_DBG	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_UPC_USB2_DBG	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_VITC_USB2_DBG	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_FTCAM_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_FTCAM_DATA	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_DFR_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_DFR_DATA	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_D2R	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_R2D	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_D2R	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_R2D	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_D2R	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_R2D	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_CLKREQ	GROUND	DEFAULT
PANEL_LPDP_DATA	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PANEL_LPDP_AUX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
RCAL_PCIE	GROUND	DEFAULT
RCAL_CIO	GROUND	DEFAULT
RCAL_MIPI	GROUND	DEFAULT
BOARD_ID	GROUND	DEFAULT
BOARD_REV	GROUND	DEFAULT
WIRELESS_TIME_SYNC	GROUND	DEFAULT
KBD_PWM	GROUND	DEFAULT
AUDIO_CONN_HEADPHONE_OUT	GROUND	DEFAULT
AUDIO_CONN_RETURN	GROUND	DEFAULT
AUDIO_CONN_SENSE	GROUND	DEFAULT
SPEAKERAMP_OUTPUT	GROUND	DEFAULT
SENSE_DIFF	GROUND	DEFAULT
SOC_XTAL_24M_IN	GROUND	DEFAULT
SOC_XTAL_24M_OUT	GROUND	DEFAULT
POWER	GROUND	DEFAULT

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	POWER	DEFAULT
SPI	POWER	DEFAULT
SPMI	POWER	DEFAULT
SWD	POWER	DEFAULT
JTAG	POWER	DEFAULT
CLOCK_24M	POWER	DEFAULT
CLOCK_32K	POWER	DEFAULT
TDM_LEFT	POWER	DEFAULT
TDM_RIGHT	POWER	DEFAULT
TDM_CODEC	POWER	DEFAULT
SPKR_ICC	POWER	DEFAULT
UART	POWER	DEFAULT
RESETS	POWER	DEFAULT
WDOG	POWER	DEFAULT
SOCHOT	POWER	DEFAULT
POWER_BUTTON	POWER	DEFAULT
FAULT	POWER	DEFAULT
DMIC_PDM	POWER	DEFAULT
FAN_CTRL	POWER	DEFAULT
USBC_SOC_BSB0_D2R_1	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB0_D2R_2	POWER	A_DIELECTRIC_7X
USBC SOC BSB0 R2D 1	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB0_R2D_2	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB0_AUX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_LSX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_D2R_1	POWER	A_DIELECTRIC_7X
USBC BSB0 CONN D2R 2	POWER	A_DIELECTRIC_7X
USBC_BSB0_CONN_R2D_1	POWER	A_DIELECTRIC_7X
USBC_BSB0_CONN_R2D_2	POWER	A_DIELECTRIC_7X
USBC_BSB0_CONN_AUXLSX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_TOP	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_BOT	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_CC	POWER	DEFAULT
USBC_UPC0_CONN_SBU	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR0_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR0_MUX_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_UPC0_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_VITC_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_D2R_1	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB1_D2R_2	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB1_R2D_1	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB1_R2D_2	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB1_AUX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_LSX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_D2R_1	POWER	A_DIELECTRIC_7X
USBC_BSB1_CONN_D2R_2	POWER	A_DIELECTRIC_7X
USBC_BSB1_CONN_R2D_1	POWER	A_DIELECTRIC_7X
USBC_BSB1_CONN_R2D_2	POWER	A_DIELECTRIC_7X
USBC_BSB1_CONN_AUXLSX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_TOP	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_BOT	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_CC	POWER	DEFAULT
USBC_UPC1_CONN_SBU	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR1_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR1_UPC1_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR_USB2_DBG	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR_MUX_USB2_DBG	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_UPC_USB2_DBG	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_VITC_USB2_DBG	POWER	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_FTCAM_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_FTCAM_DATA	POWER	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_DFR_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_DFR_DATA	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_D2R	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_R2D	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_D2R	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_R2D	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_D2R	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_R2D	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_CLKREQ	POWER	DEFAULT
PANEL_LPDP_DATA	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PANEL_LPDP_AUX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
RCAL_PCIE	POWER	DEFAULT
RCAL_CIO	POWER	DEFAULT
RCAL_MIPI	POWER	DEFAULT
BOARD_ID	POWER	DEFAULT
BOARD_REV	POWER	DEFAULT
WIRELESS_TIME_SYNC	POWER	DEFAULT
KBD_PWM	POWER	DEFAULT
AUDIO_CONN_HEADPHONE_OUT	POWER	DEFAULT
AUDIO_CONN_RETURN	POWER	DEFAULT
AUDIO_CONN_SENSE	POWER	DEFAULT
SPEAKERAMP_OUTPUT	POWER	DEFAULT
SENSE_DIFF	POWER	DEFAULT
SOC_XTAL_24M_IN	POWER	DEFAULT
SOC_XTAL_24M_OUT	POWER	DEFAULT
POWER	POWER	DEFAULT

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SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
USBC_SOC_BSB0_D2R_1	USBC_SOC_BSB0_D2R_2	A_DIELECTRIC_6X
USBC_SOC_BSB0_R2D_1	USBC_SOC_BSB0_R2D_2	A_DIELECTRIC_6X
USBC_BSB0_CONN_D2R_1	USBC_BSB0_CONN_D2R_2	A_DIELECTRIC_6X
USBC_BSB0_CONN_R2D_1	USBC_BSB0_CONN_R2D_2	A_DIELECTRIC_6X
USBC_SOC_BSB1_D2R_1	USBC_SOC_BSB1_D2R_2	A_DIELECTRIC_6X
USBC_SOC_BSB1_R2D_1	USBC_SOC_BSB1_R2D_2	A_DIELECTRIC_6X
USBC_BSB1_CONN_D2R_1	USBC_BSB1_CONN_D2R_2	A_DIELECTRIC_6X
USBC_BSB1_CONN_R2D_1	USBC_BSB1_CONN_R2D_2	A_DIELECTRIC_6X
PANEL_LPDP_DATA	PANEL_LPDP_DATA	A_DIELECTRIC_5X
SOC_XTAL_24M_IN	SOC_XTAL_24M_OUT	A_DIELECTRIC_2X

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17.2 SPACING CSETS, CLASS-CLASS

POR BOM VARIANT TABLES

DRAM VENDOR, FAB SITE, AND LEAKAGE ARE ALTERNATES IN THE SAME 639

BOM NUMBER	BOM NAME	BOM OPTIONS
639-12952	MLB1,8GB,TS-256GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_08GB,X1799_NAND_256GB_TS
639-12953	MLB1,16GB,TS-256GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_16GB,X1799_NAND_256GB_TS
639-12954	MLB1,8GB,HY-256GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_08GB,X1799_NAND_256GB_HY
639-12955	MLB1,16GB,HY-256GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_16GB,X1799_NAND_256GB_HY
639-12956	MLB1,8GB,TS-512GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_08GB,X1799_NAND_512GB_TS
639-12957	MLB1,16GB,TS-512GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_16GB,X1799_NAND_512GB_TS
639-12958	MLB1,8GB,WD-512GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_08GB,X1799_NAND_512GB_WD
639-12959	MLB1,16GB,WD-512GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_16GB,X1799_NAND_512GB_WD
639-12960	MLB1,8GB,HY-512GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_08GB,X1799_NAND_512GB_HY
639-12961	MLB1,16GB,HY-512GB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_16GB,X1799_NAND_512GB_HY
639-12962	MLB1,8GB,TS-1TB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_08GB,X1799_NAND_1TB_TS
639-12963	MLB1,16GB,TS-1TB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_16GB,X1799_NAND_1TB_TS
639-12964	MLB1,8GB,HY-1TB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_08GB,X1799_NAND_1TB_HY
639-12965	MLB1,16GB,HY-1TB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_16GB,X1799_NAND_1TB_HY
639-12966	MLB1,8GB,HY-2TB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_08GB,X1799_NAND_2TB_HY
639-12967	MLB1,16GB,HY-2TB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_16GB,X1799_NAND_2TB_HY
639-12968	MLB1,8GB,TS-2TB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_08GB,X1799_NAND_2TB_TS
639-12969	MLB1,16GB,TS-2TB,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:B0_16GB,X1799_NAND_2TB_TS

DEBUG BOM VARIANT TABLES

BOM NUMBER	BOM NAME	BOM OPTIONS
939-09328	MLB,INT-CPU,INT-SSD,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:INTERPOSER,X1799_NAND_INTERPOSER
939-09329	MLB,NO-CPU,INT-SSD,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:OFF,X1799_NAND_INTERPOSER
939-09330	MLB,INT-CPU,NO-SSD,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:INTERPOSER,X1799_NO_NAND
939-09331	MLB,NO-CPU,NO-SSD,X1799	ALT_CMN,ALTERNATE:PART,X1799_CMN_BOM,X1799_DEV_BOM,CPU:OFF,X1799_NO_NAND
939-09510	MLB,RF-TUNING,X1799	SCH,PCB,RF_CONN

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BOM VARIANT TABLES

CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-08813	1	PCBA,KANHA,X1711	U0600	CRITICAL	CPU:INTERPOSER
998-22385	1	SOC,TGA B0+8G,1Y,8C,LP,DEV,CX,M,S,M2502	U0600	CRITICAL	CPU:B0_08GB
998-22389	1	SOC,TGA B0+16G,1X,8C,LP,DEV,DX,M,S,M2502	U0600	CRITICAL	CPU:B0_16GB

NOTE: PER <RDAR://55481499>, DRAM VENDOR, FAB,SITE+ AND LEAKAGE ARE NOT CUSTOEMR FACING, SO DON'T NEED SEPARATE 639 BOMS
639 BOMS WILL SET MICRON SCK LP AS THE PRIMARY, BUT ALL OTHER COMBINATIONS ARE SET AS ALTERNATES IN THE SAME 639 BOM

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-13316	2	IC,BURNSIDE BRIDGE,USB/TB RETIMER,BGA105	UF000,UF100	CRITICAL	ATCRTMR:DEV
338S00561	2	IC,TBT,BBR,SLMN7,PRQ,A1,BGA105	UF000,UF100	CRITICAL	ATCRTMR:A1_PRQ

UPC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S02158	2	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500	CRITICAL	USBCPC:LAPTOP_B2

AMR ASSEMBLY

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-19902	1	SUBASSY (T&R) PCBA,AMR INTERPOSER,X1795	JR200	CRITICAL	AMR:X1795

TBT ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBIT5,3.0V,USON8	UF260	CRITICAL	TBT_ROM:BLANK_WINBOND
335S00232	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UF260	CRITICAL	TBT_ROM:BLANK_MACRONIX
341S01581	1	ROM,TBT/ACE (VXXXX) PRE-PROTO-1,X1740	UF260	CRITICAL	TBT_ROM:PRE_P1
341S01601	1	ROM,TBT/ACE (VXXXX) NEW, PRE-PROTO1,X1799	UF260	CRITICAL	TBT_ROM:PRE_P1_V2
341S01618	1	ROM,TBT/ACE (VXXXX), PROTO1,X1799	UF260	CRITICAL	TBT_ROM:P1
341S01672	1	ROM,TBT/ACE (VXXXX), PROTO2,X1799	UF260	CRITICAL	TBT_ROM:P2
341S01726	1	ROM,TBT/ACE (VXXXX) EVT,X1799	UF260	CRITICAL	TBT_ROM:EVT

SPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20066	1	IC,PMU,SPMU,A0,OTP-JPC,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPC
998-22526	1	IC,PMU,SPMU,A1,OTP-JPE,WLCSP196	U7700	CRITICAL	SPMU_IC:A1_JPE

MPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20064	1	IC,PMU,MPMU,A0,OTP-JPC,WLCSP440	U8100	CRITICAL	MPMU_IC:A0_DEV
998-22339	1	IC,PMU,MPMU,B0,OTP-JPE,WLCSP440	U8100	CRITICAL	MPMU_IC:B0_JPE
998-22614	1	IC,PMU,MPMU,B0,OTP-JPF,WLCSP440	U8100	CRITICAL	MPMU_IC:B0_JPF

EUSB LEVEL SHIFTER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20641	2	IC,PRT,CD2E224,B0,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_OTP6
338S00628	2	IC,PARROT,CD2E226B,B0,LSB1,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_LSB1_OTP6

CERES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-19915	1	IC,SN210V,CERES,DEV KEY,B1,SW=V7,WLCSP81	U5000	CRITICAL	SE:DEV_SW_V7
998-21255	1	IC,SN210V,B1,CERES,DEV,SW=H3,WLCSP81	U5000	CRITICAL	SE:DEV_SW_H3
338S00630	1	IC,SN210V,B1,CERES,PROD,VER=MU,WLCSP81	U5000	CRITICAL	SE:PROD_SW_MU

NAND0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,S5E MCP ROUTING STUDY,LGA110	UN000	CRITICAL	NAND0:S5E_STUDY
335S00437	1	NAND,3DV5,128GB,S5E,512G,H,SLGA110	UN000	CRITICAL	NAND0:128GB_2DP_HY
335S00462	1	NAND,3DV4,128GBT,XXX,S5E,256G,S,SLGA110	UN000	CRITICAL	NAND0:128GB_4DP_TS
335S00446	1	NAND,3DV5,128GB,S5E,256G,S,SLGA110	UN000	CRITICAL	NAND0:128GB_4DP_SS
335S00480	1	NAND,3DV4,160GBT,XXX,S5E,256G,K,SLGA110	UN000	CRITICAL	NAND0:160GB_5DP_TS
335S00438	1	NAND,3DV5,256GBT,S5E,512G,H,SLGA110	UN000	CRITICAL	NAND0:256GB_4DP_HY
335S00464	1	NAND,3DV4,256GBT,XXX,S5E,256G,T,SLGA110	UN000	CRITICAL	NAND0:256GB_8DP_TS
335S00472	1	NAND,3DV4,256GBT,XXX,S5E,256G,SD,SLGA110	UN000	CRITICAL	NAND0:256GB_8DP_WD
335S00481	1	NAND,3DV4,288GBT,XXX,S5E,256G,K,SLGA110	UN000	CRITICAL	NAND0:288GB_9DP_TS
335S00490	1	NAND,3DV4,288GBT,XXX,S5E,256G,SD,SLGA110	UN000	CRITICAL	NAND0:288GB_9DP_WD
335S00482	1	NAND,3DV5,320GBT,S5E,512G,H,SLGA110	UN000	CRITICAL	NAND0:320GB_5DP_HY
335S00439	1	NAND,3DV5,512GB,S5E,512G,H,SLGA110	UN000	CRITICAL	NAND0:512GB_8DP_HY
335S00466	1	NAND,3DV4,512GBT,XXX,S5E,256G,T,SLGA110	UN000	CRITICAL	NAND0:512GB_16DP_TS
335S00483	1	NAND,3DV5,576GBT,S5E,512G,H,SLGA110	UN000	CRITICAL	NAND0:576GB_9DP_HY
335S00468	1	NAND,3DV4,1TBT,XXX,S5E,512G,T,SLGA110	UN000	CRITICAL	NAND0:1TB_16DP_TS
335S00458	1	NAND,3DV5,1024GBT,S5E,512G,H,SLGA110	UN000	CRITICAL	NAND0:1TB_16DP_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN000	CRITICAL	NAND0:INTERPOSER

NAND1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,S5E MCP ROUTING STUDY,LGA110	UN100	CRITICAL	NAND1:S5E_STUDY
335S00437	1	NAND,3DV5,128GB,S5E,512G,H,SLGA110	UN100	CRITICAL	NAND1:128GB_2DP_HY
335S00462	1	NAND,3DV4,128GBT,XXX,S5E,256G,S,SLGA110	UN100	CRITICAL	NAND1:128GB_4DP_TS
335S00446	1	NAND,3DV5,128GB,S5E,256G,S,SLGA110	UN100	CRITICAL	NAND1:128GB_4DP_SS
335S00480	1	NAND,3DV4,160GBT,XXX,S5E,256G,K,SLGA110	UN100	CRITICAL	NAND1:160GB_5DP_TS
335S00438	1	NAND,3DV5,256GBT,S5E,512G,H,SLGA110	UN100	CRITICAL	NAND1:256GB_4DP_HY
335S00464	1	NAND,3DV4,256GBT,XXX,S5E,256G,T,SLGA110	UN100	CRITICAL	NAND1:256GB_8DP_TS
335S00472	1	NAND,3DV4,256GBT,XXX,S5E,256G,SD,SLGA110	UN100	CRITICAL	NAND1:256GB_8DP_WD
335S00481	1	NAND,3DV4,288GBT,XXX,S5E,256G,K,SLGA110	UN100	CRITICAL	NAND1:288GB_9DP_TS
335S00490	1	NAND,3DV4,288GBT,XXX,S5E,256G,SD,SLGA110	UN100	CRITICAL	NAND1:288GB_9DP_WD
335S00482	1	NAND,3DV5,320GBT,S5E,512G,H,SLGA110	UN100	CRITICAL	NAND1:320GB_5DP_HY
335S00439	1	NAND,3DV5,512GB,S5E,512G,H,SLGA110	UN100	CRITICAL	NAND1:512GB_8DP_HY
335S00466	1	NAND,3DV4,512GBT,XXX,S5E,256G,T,SLGA110	UN100	CRITICAL	NAND1:512GB_16DP_TS
335S00483	1	NAND,3DV5,576GBT,S5E,512G,H,SLGA110	UN100	CRITICAL	NAND1:576GB_9DP_HY
335S00468	1	NAND,3DV4,1TBT,XXX,S5E,512G,T,SLGA110	UN100	CRITICAL	NAND1:1TB_16DP_TS
335S00458	1	NAND,3DV5,1024GBT,S5E,512G,H,SLGA110	UN100	CRITICAL	NAND1:1TB_16DP_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN100	CRITICAL	NAND1:INTERPOSER

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BOM OPTION TABLES

COMMON BOM GROUPS

BOM GROUP	BOM OPTIONS
X1799_COMMON_PARTS	SCH,PCB,ALT_CMN,COMMON,ALTERNATE:PART,X1799_GROUP1,X1799_GROUP2,X1799_GROUP3,X1799_GROUP4,X1799_GROUP5
X1799_GROUP1	ATCRTMR:A1_PRQ,USBCPC:LAPTOP_B2,EUSB_LS:B0_LSB1_OTP6,WIFI:DEV_ES6P1,AMR:X1795,TBT_ROM:EVT,P3V8AON_IC:A1_R0B0
X1799_GROUP2	BLC_BEN_IC:V7,BLC_KBD_BOOST_USED:YES,BLC_LEDS_PER_STRING:16,BLC_5V_SERIES:10_OHM,BLC_5V_CAP:4P7_UF,CLIP:YES,CLIP_SMALL:YES
X1799_GROUP3	BOARD_REV3,BOARD_REV1,BOOT_CONFIG2,BOARDID2,SE:PROD_SW_MU,WIFI:MUR_ES6P1,PBUS_3S,RF_CONN,SSD_2L,NAND
X1799_GROUP4	SPMU_IC:A1_JPE,MPMU_IC:B0_JPF,UPC_ATCRTMR_INT,UPC_EUSBLS_INT,SLED:YES,FENCE_USBC_C770,FENCE_COMBO,FENCE_SPMU_C770
X1799_GROUP5	P1V2_PREREG:BUCK14,SECDIS_EXT_CLK,KBD_NEW,DISPLAY:P1,IPD_PMU_GPIO:EVT,P3V8AON_LPM,DMIC_CLK_33OHM

DEV BOM GROUPS

BOM GROUP	BOM OPTIONS
X1799_DEV_PARTS1	DBG_FAN,WLBT_DBG,USBC_DBG,DEBUG_BUTTON,SYS_DET_BTN,DBG_LED,SENSOR_IMU
X1799_DEV_PARTS2	DBG_VMAINISNS,VITAMIN-C:YES,SNSRES_DEV,CHGR_DBG

NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
X1799_NAND_256GB_TS	NAND0:160GB_5DP_TS,NAND1:128GB_4DP_TS
X1799_NAND_256GB_HY	NAND0:128GB_2DP_HY,NAND1:128GB_2DP_HY
X1799_NAND_512GB_TS	NAND0:288GB_9DP_TS,NAND1:256GB_8DP_TS
X1799_NAND_512GB_WD	NAND0:288GB_9DP_WD,NAND1:256GB_8DP_WD
X1799_NAND_512GB_HY	NAND0:320GB_5DP_HY,NAND1:256GB_4DP_HY
X1799_NAND_1TB_TS	NAND0:512GB_16DP_TS,NAND1:512GB_16DP_TS
X1799_NAND_1TB_HY	NAND0:576GB_9DP_HY,NAND1:512GB_8DP_HY
X1799_NAND_2TB_TS	NAND0:1TB_16DP_TS,NAND1:1TB_16DP_TS
X1799_NAND_2TB_HY	NAND0:1TB_16DP_HY,NAND1:1TB_16DP_HY
X1799_NAND_INTERPOSER	NAND0:INTERPOSER,NAND1:INTERPOSER
X1799_NO_NAND	NAND0:OFF,NAND1:OFF

SYSTEM PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-05399	1	SCHEM,COFFEE,X1799	SCH	CRITICAL	SCH
820-02020	1	PCBF,MLB,X1799	PCB	CRITICAL	PCB
685-00341	1	COMMON PARTS,MLB,X1799	COMMON_PARTS	CRITICAL	X1799_CMN_BOM
985-01178	1	DEV PARTS,MLB,X1799	DEV_PARTS	CRITICAL	X1799_DEV_BOM

COMMON PARTS BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00341	COMMON PARTS,MLB,X1799	X1799_COMMON_PARTS

DEV PARTS BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
985-01178	DEV PARTS,MLB,X1799	X1799_DEV_PARTS1,X1799_DEV_PARTS2

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BOM GROUPS

SYSTEM EE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01346	353S01320	ALT_CMN	ALL	<RDAR://56390543>
376S1080	376S0820	ALT_CMN	ALL	<RDAR://57125638>
107S0276	107S00020	ALT_CMN	ALL	<RDAR://57126636>
311S00176	311S00153	ALT_CMN	ALL	<RDAR://57133089>
353S02030	353S01993	ALT_CMN	ALL	<RDAR://57133661>
138S00284	138S00136	ALT_CMN	ALL	<RDAR://57134599>
132S00229	132S00010	ALT_CMN	ALL	<RDAR://57135129>
107S00346	107S00116	ALT_CMN	ALL	<RDAR://57135567>
138S0852	138S0818	ALT_CMN	ALL	<RDAR://57137990>
138S0750	138S00097	ALT_CMN	ALL	<RDAR://57138474>
152S00864	152S00851	ALT_CMN	ALL	<RDAR://57159654>
138S00181	138S0835	ALT_CMN	ALL	<RDAR://57161300>
138S00291	138S0835	ALT_CMN	ALL	<RDAR://57161300>
376S1137	376S00019	ALT_CMN	ALL	<RDAR://57166351>
311S00156	311S00129	ALT_CMN	ALL	<RDAR://57167823>
376S00224	376S00282	ALT_CMN	ALL	<RDAR://57168696>
376S1128	376S00282	ALT_CMN	ALL	<RDAR://57168696>
311S00060	311S0273	ALT_CMN	ALL	<RDAR://57172430>
353S00878	353S00599	ALT_CMN	ALL	<RDAR://57173083>
371S00220	371S00181	ALT_CMN	ALL	<RDAR://57196734>
376S00146	376S1061	ALT_CMN	ALL	<RDAR://57198167>
311S00013	311S0508	ALT_CMN	ALL	<RDAR://57211339>
197S00046	197S00036	ALT_CMN	ALL	<RDAR://57229594>
197S00047	197S00036	ALT_CMN	ALL	<RDAR://57229594>
197S00048	97S00036	ALT_CMN	ALL	<RDAR://57229594>
377S0155	3 7S0184	ALT_CMN	ALL	<RDAR://57230484>
353S02358	353S4262	ALT_CMN	ALL	<RDAR://57812391>
353S02361	353S02314	ALT_CMN	ALL	<RDAR://57807324>
353S02406	353S02211	ALT_CMN	ALL	<RDAR://59230338>
353S02408	353S02214	ALT_CMN	ALL	<RDAR://59230141>
311S00268	311S00246	ALT_CMN	ALL	<RDAR://58875763>
155S00018	155S0664	ALT_CMN	ALL	<RDAR://58883322>
155S0823	155S0644	ALT_CMN	ALL	<RDAR://58885574>
138S00264	138S00008	ALT_CMN	ALL	<RDAR://58886526>
155S0914	155S0897	ALT_CMN	ALL	<RDAR://58926571>
155S00190	155S0897	ALT_CMN	ALL	<RDAR://58926571>
155S0660	155S0513	ALT_CMN	ALL	<RDAR://58929661>
155S0694	155S0387	ALT_CMN	ALL	<RDAR://58930067>
152S00434	2S1829	ALT_CMN	ALL	<RDAR://58931541>
138S00229	138S00107	ALT_CMN	ALL	<RDAR://58936780>
132S00064	132S0409	ALT_CMN	ALL	<RDAR://58939796>
138S00116	138S00071	ALT_CMN	ALL	<RDAR://58939873>
138S00117	138S00071	ALT_CMN	ALL	<RDAR://58939873>
138S0715	138S0732	ALT_CMN	ALL	<RDAR://58961735>
138S00104	38S0978	ALT_CMN	ALL	<RDAR://58970274>
138S00084	138S00060	ALT_CMN	ALL	<RDAR://58972151>
155S00034	155S0706	ALT_CMN	ALL	<RDAR://58997770>
107S0150	107S0208	ALT_CMN	ALL	<RDAR://59081387>
107S00298	107S0208	ALT_CMN	ALL	<RDAR://59081387>
377S00123	377S00031	ALT_CMN	ALL	<RDAR://59079997>
155S0275	155S00188	ALT_CMN	ALL	<RDAR://58886241>
155S00007	155S0667	ALT_CMN	ALL	<RDAR://59047420>
138S00049	138S0831	ALT_CMN	ALL	<RDAR://59079351>
138S00077	138S00035	ALT_CMN	ALL	<RDAR://59276464>
138S00093	138S00035	ALT_CMN	ALL	<RDAR://59276464>
311S00267	311S00244	ALT_CMN	ALL	<RDAR://58875407>
377S00186	377S00060	ALT_CMN	ALL	<RDAR://58939991>
138S00164	138S00138	ALT_CMN	ALL	<RDAR://61547071>
138S00280	38S00138	ALT_CMN	ALL	<RDAR://61547071>
138S00139	138S00138	ALT_CMN	ALL	<RDAR://61547071>

SYSTEM EE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1068	138S00215	ALT_CMN	ALL	<RDAR://61797939>
311S00248	311S00243	ALT_CMN	ALL	<RDAR://61794063>
311S00269	311S00234	ALT_CMN	ALL	<RDAR://58875314>
376S00292	376S1140	ALT_CMN	ALL	<RDAR://58350656>
311S0196	311S00245	ALT_CMN	ALL	<RDAR://62345781>

WIFI MODULE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00758	339S00763	ALT_CMN	ALL	

BLC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0738	138S1101	ALT_CMN	ALL	<RDAR://55465318>
138S0846	138S0811	ALT_CMN	ALL	<RDAR://55465318>
376S1053	376S0604	ALT_CMN	ALL	<RDAR://55465318>
152S00359	152S00253	ALT_CMN	ALL	<RDAR://55465318>
740S00041	740S0159	ALT_CMN	ALL	<RDAR://55465318>
371S00077	371S00180	ALT_CMN	ALL	<RDAR://55465318>
376S1106	376S0678	ALT_CMN	ALL	<RDAR://55465318>
107S00033	107S00034	ALT_CMN	ALL	<RDAR://55465318>
138S00087	138S1086	ALT_CMN	ALL	<RDAR://55465318>
152S00812	152S1701	ALT_CMN	ALL	<RDAR://55465318>
371S00217	371S00079	ALT_CMN	ALL	<RDAR://55465318>

PD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S00033	518S0867	ALT_CMN	ALL	<RDAR://60043079>
806-24548	806-24455	ALT_CMN	ALL	<RDAR://60043307>
806-24550	806-24457	ALT_CMN	ALL	<RDAR://60043307>

SOC 8G

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-22386	998-22385	ALT_CMN	ALL	<RDAR://55481499>
998-22387	998-22385	ALT_CMN	ALL	<RDAR://55481499>
998-22388	998-22385	ALT_CMN	ALL	<RDAR://55481499>
998-22393	998-22385	ALT_CMN	ALL	<RDAR://55481499>
998-22394	998-22385	ALT_CMN	ALL	<RDAR://55481499>
998-22395	998-22385	ALT_CMN	ALL	<RDAR://55481499>
998-22396	998-22385	ALT_CMN	ALL	<RDAR://55481499>

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SOC 16G

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-22390	998-22389	ALT_CMN	ALL	<RDAR://55481499>
998-22391	998-22389	ALT_CMN	ALL	<RDAR://55481499>
998-22392	998-22389	ALT_CMN	ALL	<RDAR://55481499>
998-22397	998-22389	ALT_CMN	ALL	<RDAR://55481499>
998-22398	998-22389	ALT_CMN	ALL	<RDAR://55481499>
998-22399	998-22389	ALT_CMN	ALL	<RDAR://55481499>
998-22400	998-22389	ALT_CMN	ALL	<RDAR://55481499>

DCDC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0863	138S0853	ALT_CMN	ALL	<RDAR://56380033>
152S00398	152S00204	ALT_CMN	ALL	<RDAR://56380033>
152S00963	152S00885	ALT_CMN	ALL	<RDAR://56380033>
138S00047	138S00073	ALT_CMN	ALL	<RDAR://56380033>
152S01317	152S01268	ALT_CMN	ALL	<RDAR://57328156>
107S00029	107S00087	ALT_CMN	ALL	<RDAR://56380033>
107S00055	107S00090	ALT_CMN	ALL	<RDAR://59138399>
107S00365	107S00373	ALT_CMN	ALL	<RDAR://59138399>
128S00026	128S00011	ALT_CMN	ALL	<RDAR://56380033>
128S00087	128S00011	ALT_CMN	ALL	<RDAR://56380033>
128S00031	128S00011	ALT_CMN	ALL	<RDAR://56380033>
128S00039	128S00038	ALT_CMN	ALL	<RDAR://56380033>
128S0302	128S00038	ALT_CMN	ALL	<RDAR://56380033>
128S00065	128S00067	ALT_CMN	ALL	<RDAR://56380033>
128S00094	128S00067	ALT_CMN	ALL	<RDAR://56380033>
128S0364	128S0264	ALT_CMN	ALL	<RDAR://56380033>
152S00680	152S00198	ALT_CMN	ALL	<RDAR://56380033>
152S00383	152S00198	ALT_CMN	ALL	<RDAR://56380033>
152S00708	152S00265	ALT_CMN	ALL	<RDAR://56380033>
152S00997	152S00476	ALT_CMN	ALL	<RDAR://56380033>
152S00367	152S01248	ALT_CMN	ALL	<RDAR://56380033>
376S00303	376S00012	ALT_CMN	ALL	<RDAR://56380033>
376S00204	376S00203	ALT_CMN	ALL	<RDAR://56380033>
376S00227	376S00203	ALT_CMN	ALL	<RDAR://56380033>
376S00226	376S00203	ALT_CMN	ALL	<RDAR://56380033>
376S1147	376S00281	ALT_CMN	ALL	<RDAR://59078633>
376S00007	376S1179	ALT_CMN	ALL	<RDAR://56380033>
376S00228	376S1179	ALT_CMN	ALL	<RDAR://56380033>
138S0789	138S0941	ALT_CMN	ALL	<RDAR://56380033>
107S00071	107S00053	ALT_CMN	ALL	<RDAR://56380033>
138S00332	138S00328	ALT_CMN	ALL	<RDAR://57328643>
152S00343	152S00839	ALT_CMN	ALL	<RDAR://57238826>
152S01090	152S01085	ALT_CMN	ALL	<RDAR://57230783>
740S0118	740S00028	ALT_CMN	ALL	<RDAR://58994885>
132S00012	132S0401	ALT_CMN	ALL	<RDAR://58940759>
132S00176	132S0640	ALT_CMN	ALL	<RDAR://58937688>
152S01344	152S00883	ALT_CMN	ALL	<RDAR://59451415>
116S00007	116S00006	ALT_CMN	ALL	<RDAR://59080433>
138S00330	138S00081	ALT_CMN	ALL	<RDAR://59079306>
152S00874	152S00979	ALT_CMN	ALL	<RDAR://59735030>
353S1429	353S02402	ALT_CMN	ALL	<RDAR://59746381>

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BOM ALTERNATES

PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A,SPKRAMP_B
SPKRAMP_D,SPKRAMP_E
SPKRAMP_LVL_4B_QFN
SPKRAMP_LVL_1B_SON

REF_SPKRAMP_TAS5770

J293 HAS 4 AMPS, 2 LEFT AND 2 RIGHT.
LEFT ARE A, B. RIGHT ARE D, E.
USE SAME LEVEL SHIFTERS AS TRACKPAD SPI
USE 1.2V BUFFER WITH 1.8V CAPABLE INPUT AS 1.8 TO 1.2 LEVEL SHIFTER

PACK_OPTIONS TO INCLUDE IN NETLIST
CHGR_60W
CHGR_TP_TOP,CHGR_TP_BOT,CHGR_TP

REF_CHARGER_SUONA

J293'S CHARGER IS B379 WHICH IS 61W, SO WE USE
60-100W OPTION PER REF CHARGER SUONA CONFIG TABLE
ENABLE ALL CHARGER TEST POINTS

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_SPI_UPC0
USBC_DEBUG_UPC0
USBC_LAPTOP
USBC01_VR5V_LOCAL_NO
PKGS:SMALL_PITCH

REF_USBC_ACE2

SET SPI UPC TO BE 0, BACK LEFT
SET DEBUG UPC TO BE 0, BACK LEFT
ENABLE PORTS FOR CHARGING
LEAVE ACE2 5V ENABLE GPIOS SEPARATE, AS 5V DEDICATED LOCAL VR NOT USED
ENABLE SMALL PITCH PARTS ON USBC PAGES (OTHER PROJECTS USING BIGGER PITCH OPTIONS)

PACK_OPTIONS TO INCLUDE IN NETLIST
FTCAM
DFR
80UM_STEN
SMALL_NOR

REF_SOC_H13G

J293 HAS A FTCAM, SO TURN ON FTCAM MIPI REXT RESISTOR
J293 HAS A DFR, SO TURN ON DFR MIPI REXT RESISTOR
J293 WILL USE 80 UM TOP SIDE STENCIL FOR SOC BYPASS CAPS
SMALL NOR IS 4X3 SINGLE SOURCE PACKAGE, LARGE NOR IS 4X4 PACKAGE WITH MULTIPLE ALTERNATES

PACK_OPTIONS TO INCLUDE IN NETLIST
JTAG_SECDIS:YES
PROTO_PULLDOWN_SECDIS
PROD_SECDIS

REF_SECDIS_SAK

KEEP THE JTAG CONNECTOR AND DEBUG PULLS
PULL DOWN SEP OUTPUTS WHEN SYSTEM IS IN S2 OR BELOW
ALL PRODUCTION SYSTEMS CALL OUT PROD_SECDIS

PACK_OPTIONS TO INCLUDE IN NETLIST
AMR_INTERPOSER_LEFT
NO_AMR_INTERPOSER_RIGHT

REF_SECDIS_AMR

ON J293, THE LEFT AMR IS ON THE MLB, SO CALL OUT AMR_INTERPOSER_LEFT
1M PULL DOWNS ON RIGHT SIDE ENABLED WITH NO_AMR_INTERPOSER_RIGHT, TO ENSURE
NET IS LOW WHEN NO FLEX IS INSTALLED FOR THE RIGHT SIDE

PACK_OPTIONS TO INCLUDE IN NETLIST
IPEX
WLBT_DBG_CONN

REF_WIRELESS_RASPUTIN

3X_ANTENNA PACK OPTION IS FOR PROGRAMS WITH DEDICATED BT ANTENNA, WHICH
J293 DOES NOT HAVE, SO THIS IS NOT CALLED OUT
J293 USES IPEX CONNECTOR (NOT SUNWAY) FOR ANTENNA CONNECTOR, SO CALL OUT IPEX
J293 USES THE DEBUG WIFI CONNECTOR, SO WLBT_DBG_CONN IS CALLED OUT

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PACK_OPTIONS TO INCLUDE IN NETLIST
3V3_S2_PBUS-D2

REF_VR_3V3_TPS62135

SETTING D2 CAP SIZE

PACK_OPTIONS TO INCLUDE IN NETLIST
5V_S2_PBUS-D2

REF_VR_5V_LT8642S

SETTING D2 CAP SIZE

PACK_OPTIONS TO INCLUDE IN NETLIST
3V8_AON_PBUS-D2
3V8_AON_I2C-DEV
3V8_EXT_DIODE

REF_VR_ICEMAN

SETTING D2 CAP SIZE
SHORT I2C TO GND FOR POR
ENABLE EXTERNAL CHARGE PUMP DIODES

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CHECKPLUS WAIVES

8 85 82 B1 I2C_KBD_SDA
CKPLUS_WAIVE=I2C_PULLUP

89 85 82 B1 I2C_KBD_SCL
CKPLUS_WAIVE=I2C_PULLUP

24 B1 I2C_P3V8AON_SDA
CKPLUS_WAIVE=I2C_PULLUP

24 B1 I2C_P3V8AON_SCL
CKPLUS_WAIVE=I2C_PULLUP

SYNC_MASTER=T660_MLB SYNC_DATE=08/20/2010

CHECKPLUS SUPPORT